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April 1st, 2010
Renesas Electronics Corporation

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1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and are packaged in a 52-pin molded-plastic LQFP or a 64-pin molded-plastic FLGA. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.
Furthermore, the R8C/25 Group has on-chip data flash (1 KB x 2 blocks).
The difference between the R8C/24 Group and R8C/25 Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/24 Group and Table 1.2 outlines the Functions and Specifications for R8C/25 Group.

Table 1.1 Functions and Specifications for R8C/24 Group

Item			Specification
CPU	Number of fundamental instructions		89 instructions
	Minimum instruction execution time		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
	Operating mode		Single-chip
	Address space		1 Mbyte
	Memory capacity		Refer to **Table 1.3 Product Information for R8C/24 Group**
Peripheral Functions	Ports		I/O ports: 41 pins, Input port: 3 pins
	LED drive ports		I/O ports: 8 pins
	Timers		Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits × 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interfaces		2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface		1 channel I²C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module		Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter		10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer		15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts		Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz)
			Real-time clock (timer RE)
	Oscillation stop detection function		XIN clock oscillation stop detection function
	Voltage detection circuit		On-chip
	Power-on reset circuit		On-chip
Electrical Characteristics	Supply voltage		VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz)
	Current consumption		Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage		VCC = 2.7 to 5.5 V
	Programming and erasure endurance		100 times
Operating Ambient Temperature			-20 to 85°C (N version)
			-40 to 85°C (D version)(2)
			-20 to 105°C (Y version)(3)
Package			52-pin molded-plastic LQFP
			64-pin molded-plastic FLGA

NOTES:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

Table 1.2 Functions and Specifications for R8C/25 Group

Item			Specification
CPU	Number of fundamental instructions		89 instructions
	Minimum instruction execution time		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
	Operating mode		Single-chip
	Address space		1 Mbyte
	Memory capacity		Refer to **Table 1.4 Product Information for R8C/25 Group**
Peripheral Functions	Ports		I/O ports: 41 pins, Input port: 3 pins
	LED drive ports		I/O ports: 8 pins
	Timers		Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits × 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interface		2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface		1 channel I2C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module		Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter		10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer		15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts		Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz)
			Real-time clock (timer RE)
	Oscillation stop detection function		XIN clock oscillation stop detection function
	Voltage detection circuit		On-chip
	Power-on reset circuit		On-chip
Electrical Characteristics	Supply voltage		VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz)
	Current consumption		Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash memory	Programming and erasure voltage		VCC = 2.7 to 5.5 V
	Programming and erasure endurance		1,0000 times (data flash)
			1,000 times (program ROM)
Operating Ambient Temperature			-20 to 85°C (N version)
			-40 to 85°C (D version)(2)
			-20 to 105°C (Y version)(3)
Package			52-pin molded-plastic LQFP
			64-pin molded-plastic FLGA

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

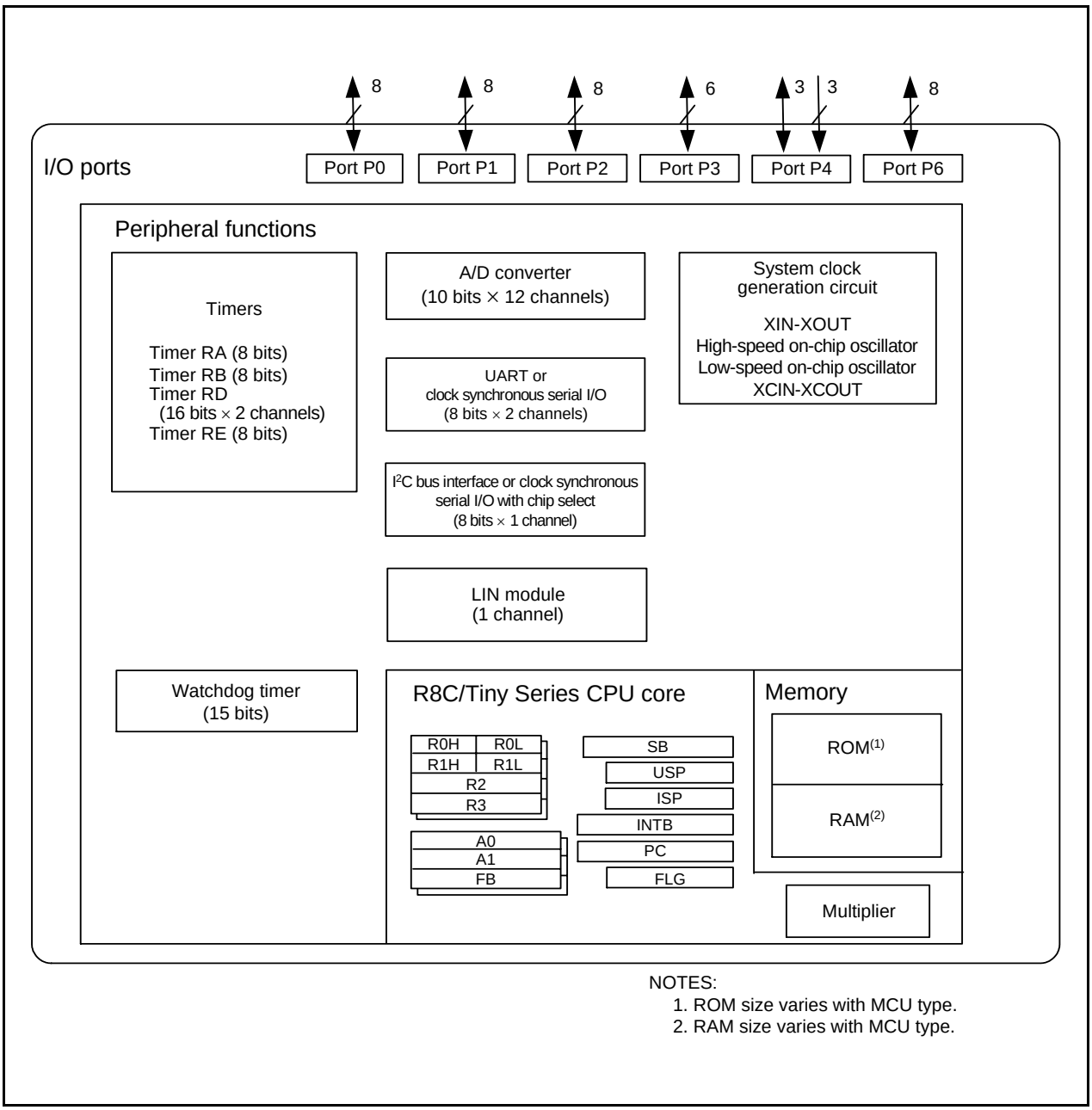


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information for R8C/24 Group and Table 1.4 lists the Product Information for R8C/25 Group.

Table 1.3 Product Information for R8C/24 Group **Current of Feb. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21244SNFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21245SNFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	
R5F21244SDFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21245SDFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21245SNXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNXXXLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	
R5F21244SDXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21245SDXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

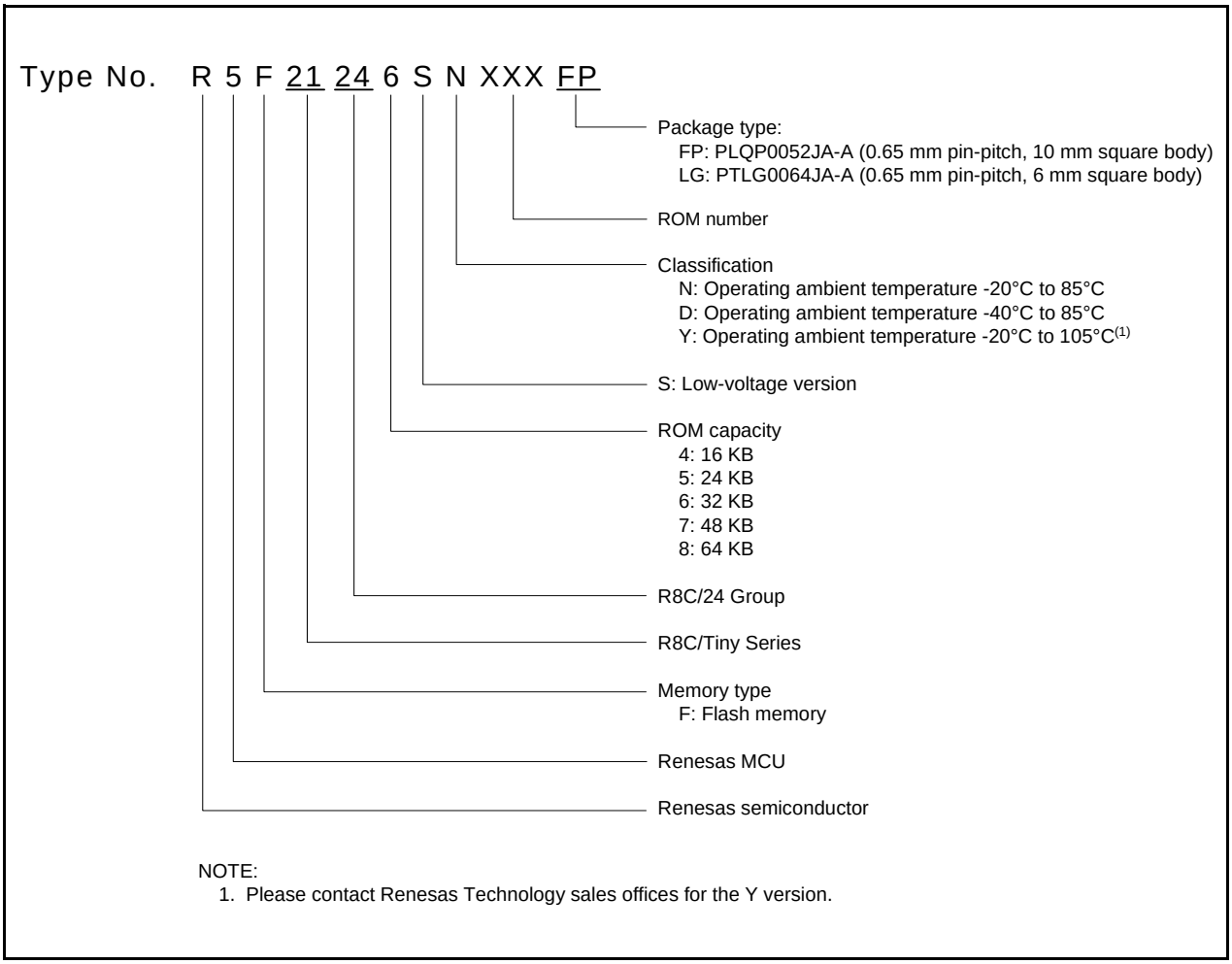


Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group

Table 1.4 Product Information for R8C/25 Group Current of Feb. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21254SNFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21255SNFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21255SDFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21255SNXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNXXXLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21255SDXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

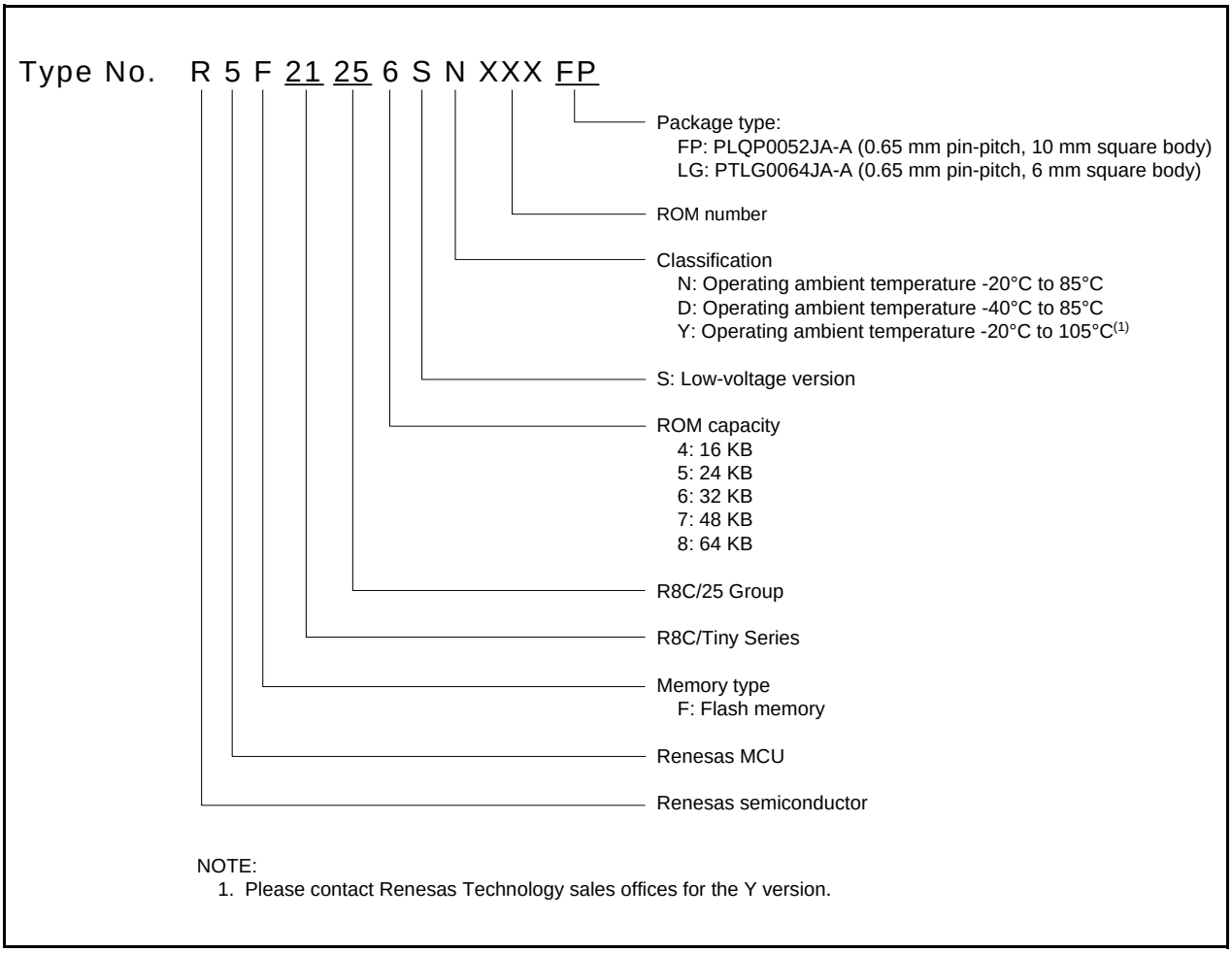
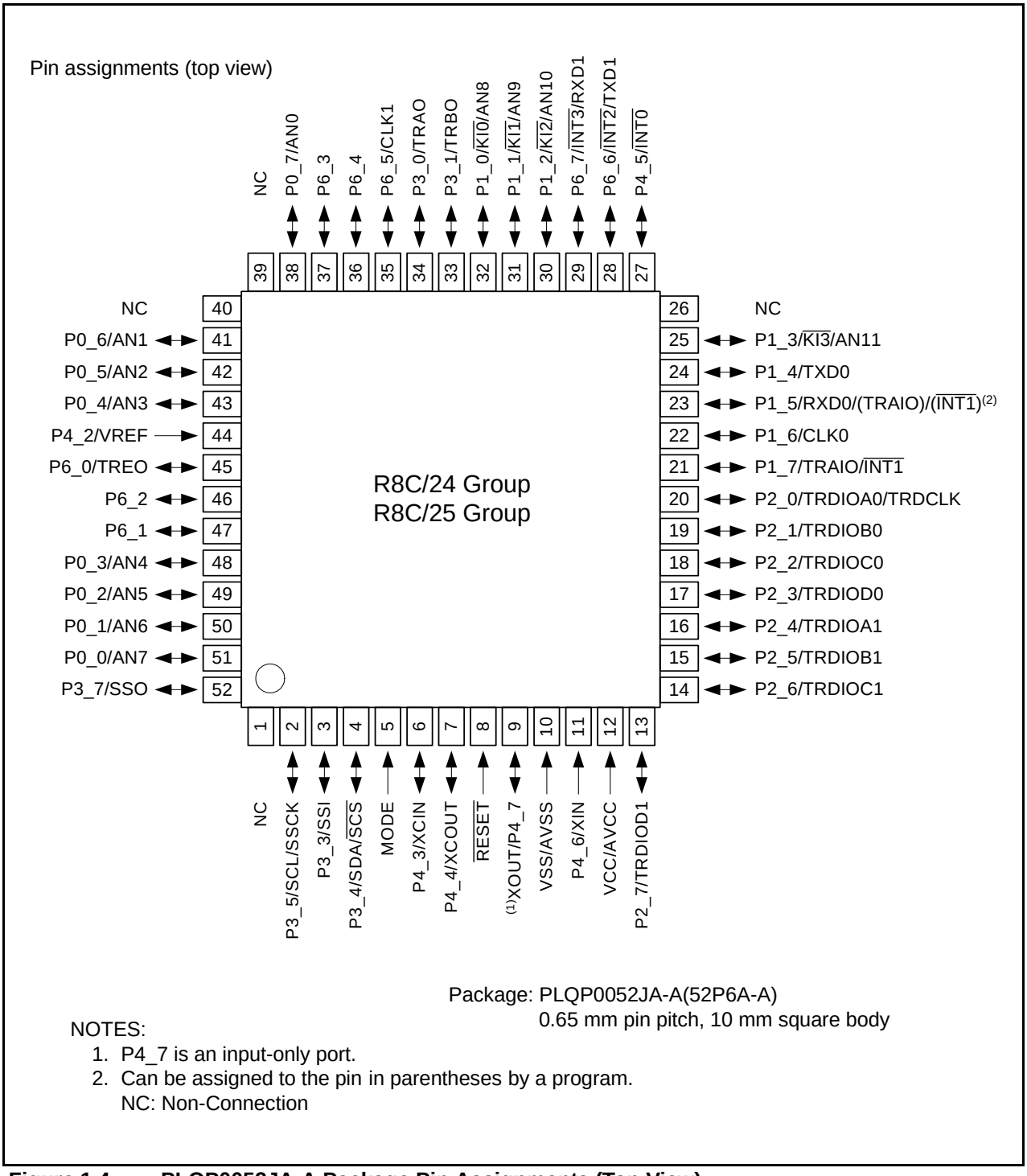


Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group

1.5 Pin Assignments

Figure 1.4 shows PLQP0052JA-A Package Pin Assignments (Top View). Figure 1.5 shows PTLG0064JA-A Package Pin Assignments.



Package: PLQP0052JA-A(52P6A-A)
0.65 mm pin pitch, 10 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
   NC: Non-Connection

Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View)

Pin assignments (top perspective view)

	A	B	C	D	E	F	G	H	
8	3 P3_3/SSI	50 P0_1/AN6	48 P0_3/AN4	46 P6_2	45 P6_0/TREO	NC	36 P6_4	NC	8
7	4 P3_4/SDA/$\overline{\text{SCS}}$	51 P0_0/AN7	49 P0_2/AN5	NC	44 P4_2/VREF	34 P3_0/TRAO	35 P6_5/CLK1	NC	7
6	NC	5 MODE	52 P3_7/SSO	47 P6_1	43 P0_4/AN3	42 P0_5/AN2	NC	33 P3_1/TRBO	6
5	7 P4_4/XCOUT	NC	6 P4_3/XCIN	2 P3_5/SCL/SSCK	37 P6_3	NC	41 P0_6/AN1	38 P0_7/AN0	5
4	13 P2_7/TRDIOD1	12 VCC/AVCC	NC	9 XOUT/P4_7(1)	8 $\overline{\text{RESET}}$	32 P1_0/$\overline{\text{KI0}}$/AN8	31 P1_1/$\overline{\text{KI1}}$/AN9	NC	4
3	NC	10 VSS/AVSS	16 P2_4/TRDIOA1	19 P2_1/TRDIOB0	23 P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2)	NC	NC	30 P1_2/$\overline{\text{KI2}}$/AN10	3
2	NC	11 XIN/P4_6	17 P2_3/TRDIOD0	20 P2_0/TRDIOA0/TRDCLK	NC	24 P1_4/TXD0	28 P6_6/$\overline{\text{INT2}}$/TXD1	NC	2
1	14 P2_6/TRDIOC1	15 P2_5/TRDIOB1	18 P2_2/TRDIOC0	21 P1_7/TRAIO/$\overline{\text{INT1}}$	22 P1_6/CLK0	25 P1_3/$\overline{\text{KI3}}$/AN11	27 P4_5/$\overline{\text{INT0}}$	29 P6_7/$\overline{\text{INT3}}$/RXD1	1
	A	B	C	D	E	F	G	H	

Package: PTLG0064JA-A(64F0G)
0.65 mm pin pitch, 6 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. In the figure, the numbers in circles are the pin numbers of the 52-pin LQFP package (PLQP0052JA-A).
   NC: Non-Connection

R5F21244S
NLG
JAPAN

Pin assignments (top view)

Figure 1.5 PTLG0064JA-A Package Pin Assignments

1.6 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins. To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RD input pin. $\overline{\text{INT1}}$ is timer RA input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O ports
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Serial interface	CLK0, CLK1	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	O	Serial data output pins
I^2C bus interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Clock synchronous serial I/O with chip select	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

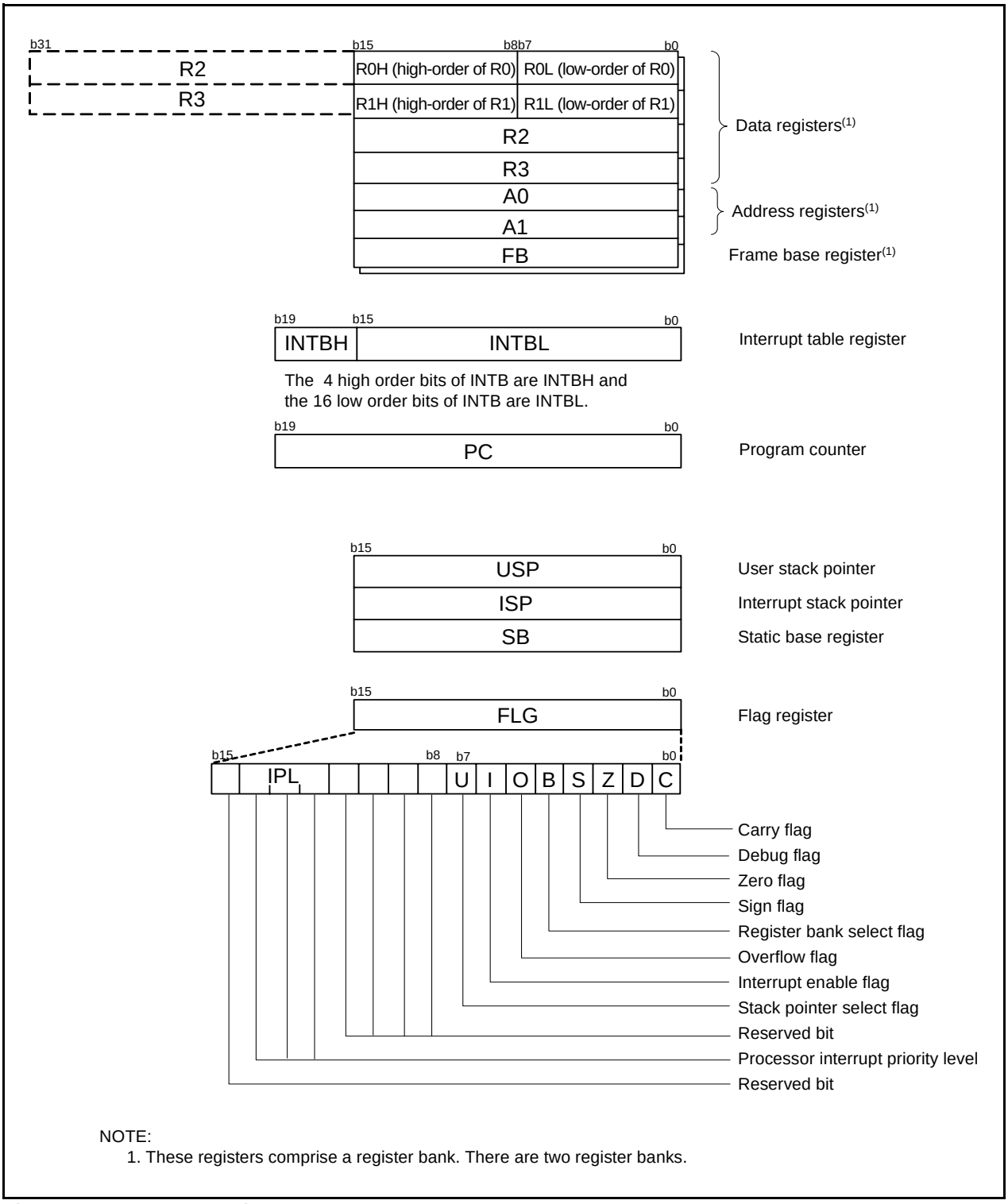
Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C bus Interface	A/D Converter
2		P3_5				SSCK	SCL	
3		P3_3				SSI		
4		P3_4				$\overline{SCS}$	$\overline{SDA}$	
5	MODE							
6	XCIN	P4_3						
7	XCOUT	P4_4						
8	$\overline{RESET}$							
9	XOUT	P4_7						
10	VSS/AVSS							
11	XIN	P4_6						
12	VCC/AVCC							
13		P2_7		TRDIOD1				
14		P2_6		TRDIOC1				
15		P2_5		TRDIOB1				
16		P2_4		TRDIOA1				
17		P2_3		TRDIOD0				
18		P2_2		TRDIOC0				
19		P2_1		TRDIOB0				
20		P2_0		TRDIOA0/TRDCLK				
21		P1_7	$\overline{INT1}$	TRAIO				
22		P1_6			CLK0			
23		P1_5	$\overline{(INT1)}$(1)	(TRAIO)(1)	RXD0			
24		P1_4			TXD0			
25		P1_3	$\overline{KI3}$					AN11
27		P4_5	$\overline{INT0}$	$\overline{INT0}$				
28		P6_6	$\overline{INT2}$		TXD1			
29		P6_7	$\overline{INT3}$		RXD1			
30		P1_2	$\overline{KI2}$					AN10
31		P1_1	$\overline{KI1}$					AN9
32		P1_0	$\overline{KI0}$					AN8
33		P3_1		TRBO				
34		P3_0		TRAO				
35		P6_5			CLK1			
36		P6_4						
37		P6_3						
38		P0_7						AN0
41		P0_6						AN1
42		P0_5						AN2
43		P0_4						AN3
44	VREF	P4_2						
45		P6_0		TREO				
46		P6_2						
47		P6_1						
48		P0_3						AN4
49		P0_2						AN5
50		P0_1						AN6
51		P0_0						AN7
52		P3_7				SSO		

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

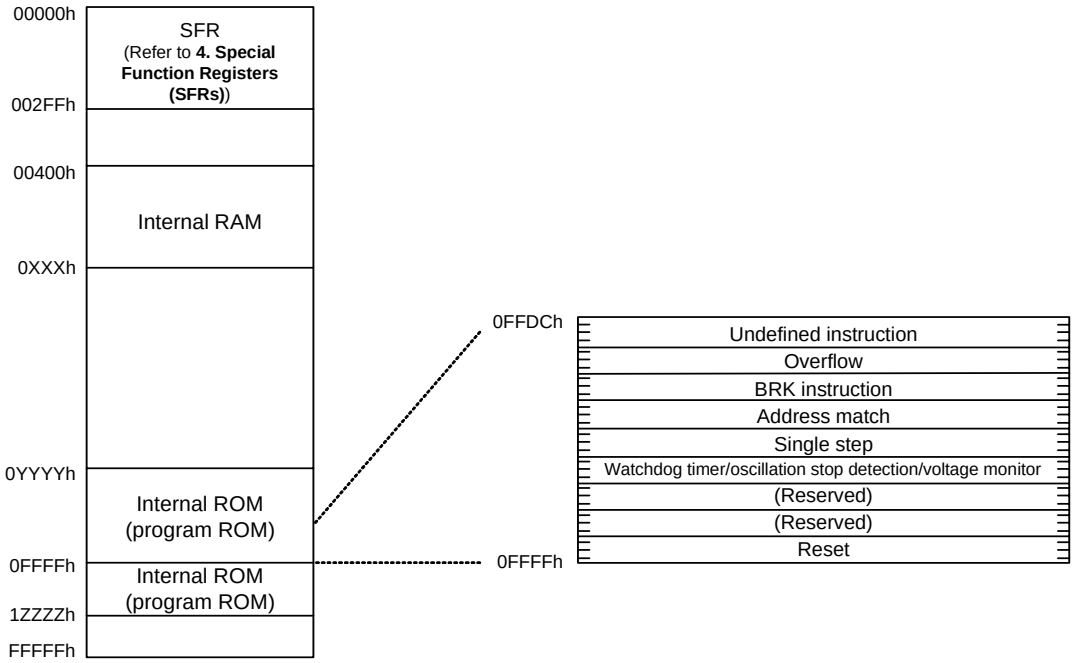
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/24 Group

Figure 3.1 is a Memory Map of R8C/24 Group. The R8C/24 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM area is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



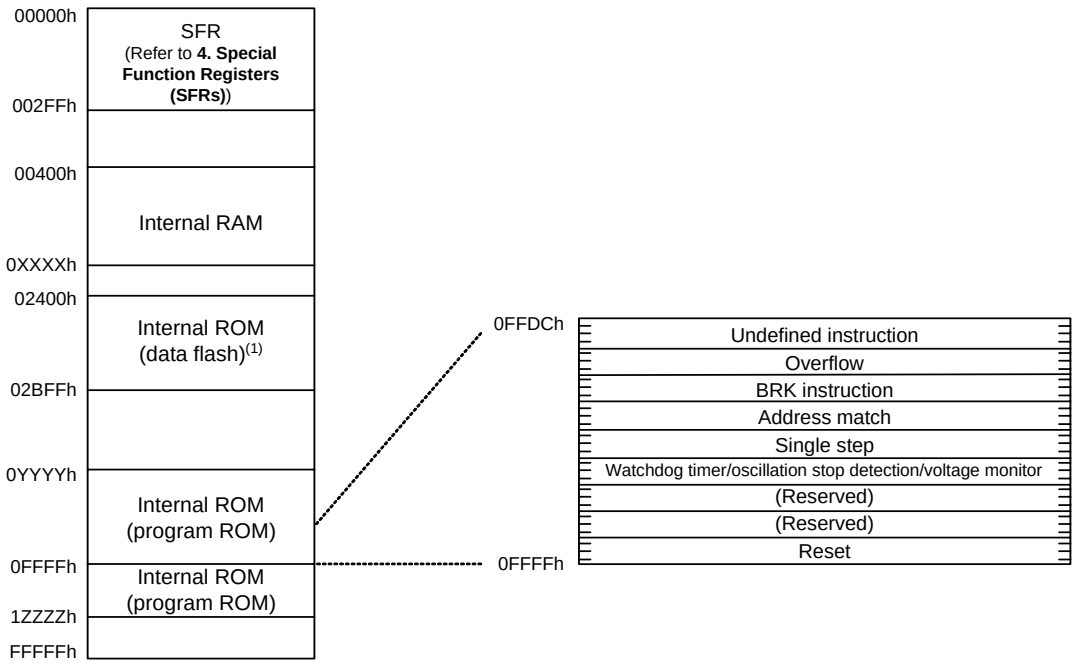
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21244SNFP, R5F21244SNXXXFP, R5F21244SDFP, R5F21244SDXXXFP, R5F21244SNLG, R5F21244SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21245SNFP, R5F21245SNXXXFP, R5F21245SDFP, R5F21245SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21246SNFP, R5F21246SNXXXFP, R5F21246SDFP, R5F21246SDXXXFP, R5F21246SNLG, R5F21246SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21247SNFP, R5F21247SNXXXFP, R5F21247SDFP, R5F21247SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21248SNFP, R5F21248SNXXXFP, R5F21248SDFP, R5F21248SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.1 Memory Map of R8C/24 Group

3.2 R8C/25 Group

Figure 3.2 is a Memory Map of R8C/25 Group. The R8C/25 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21254SNFP, R5F21254SNXXXFP, R5F21254SDFP, R5F21254SDXXXFP, R5F21254SNLG, R5F21254SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21255SNFP, R5F21255SNXXXFP, R5F21255SDFP, R5F21255SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21256SNFP, R5F21256SNXXXFP, R5F21256SDFP, R5F21256SDXXXFP, R5F21256SNLG, R5F21256SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21257SNFP, R5F21257SNXXXFP, R5F21257SDFP, R5F21257SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21258SNFP, R5F21258SNXXXFP, R5F21258SDFP, R5F21258SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.2 Memory Map of R8C/25 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b[6]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 00100000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[5]	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register[2]	VW0C	0000X000b[3] 0100X001b[4]
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset.
5. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC Interrupt Control Register[2]	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)[1]

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H / IIC bus Control Register 1[2]	SSCRH / ICCR1	00h
00B9h	SS Control Register L / IIC bus Control Register 2[2]	SSCRL / ICCR2	01111101b
00BAh	SS Mode Register / IIC bus Mode Register[2]	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register[2]	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register[2]	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register[2]	SSMR2 / SAR	00h
00BEh	SS Transmit Data Register / IIC bus Transmit Data Register[2]	SSTDR / ICDRT	FFh
00BFh	SS Receive Data Register / IIC bus Receive Data Register[2]	SSRDR / ICDRR	FFh

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)[1]

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

The electrical characteristics of N version (Topr = -20 to 85°C) and D version (Topr = -40 to 85°C) are listed below.
Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = -20 to 105°C).

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC} + 0.3	V
V_O	Output voltage		-0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_{opr} = 25°C	500(1)	mW
T_{opr}	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

NOTE:
1. 300 mW for the PTLG0064JA-A package.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.2	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	-160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	-80	mA
$I_{OH(peak)}$	Peak output “H” current	Except P2_0 to P2_7		–	–	-10	mA
		P2_0 to P2_7		–	–	-40	mA
$I_{OH(avg)}$	Average output “H” current	Except P2_0 to P2_7		–	–	-5	mA
		P2_0 to P2_7		–	–	-20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output “L” current	Except P2_0 to P2_7		–	–	10	mA
		P2_0 to P2_7		–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Except P2_0 to P2_7		–	–	5	mA
		P2_0 to P2_7		–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency		2.2 V ≤ V_{CC} ≤ 5.5 V	0	–	70	kHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V_{CC} ≤ 5.5 V	–	–	5	MHz

NOTES:
1. V_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}	–	–	10	Bit
–	Absolute accuracy	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 3.3 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 3.3 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 5 MHz, V_{ref} = AV_{CC} = 2.2 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 5 MHz, V_{ref} = AV_{CC} = 2.2 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = AV_{CC}	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage(2)			0	–	AV_{CC}	V
–	A/D operating clock frequency	Without sample and hold	V_{ref} = AV_{CC} = 2.7 to 5.5 V	0.25	–	10	MHz
		With sample and hold	V_{ref} = AV_{CC} = 2.7 to 5.5 V	1	–	10	MHz
		Without sample and hold	V_{ref} = AV_{CC} = 2.2 to 5.5 V	0.25	–	5	MHz
		With sample and hold	V_{ref} = AV_{CC} = 2.2 to 5.5 V	1	–	5	MHz

NOTES:
1. AV_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

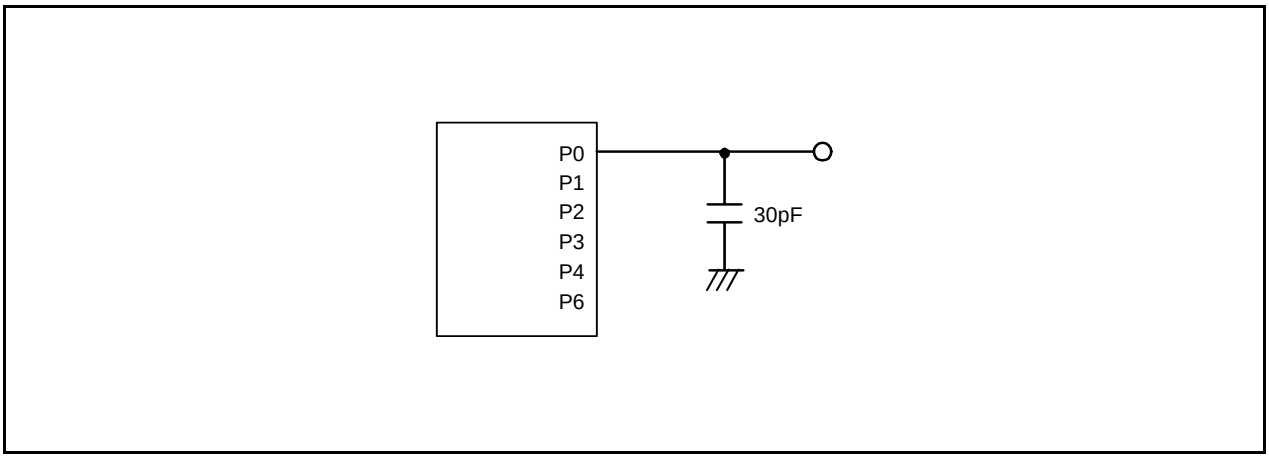


Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/24 Group	100(3)	–	–	times
		R8C/25 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

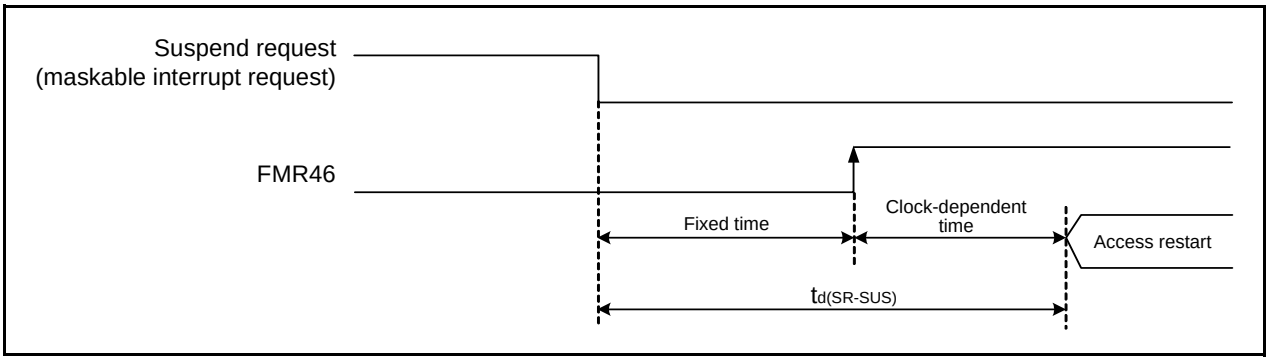


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics

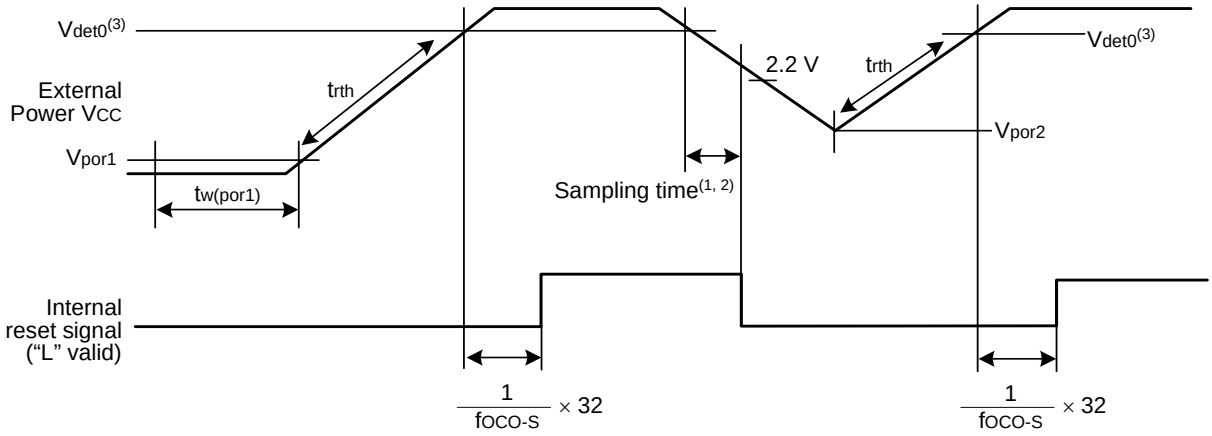
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V_{det0}	V
t_{rth}	External power V_{CC} rise gradient(2)		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 to 5.25 V 0°C ≤ T_{opr} ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	38.8	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C	38.4	40	40.8	MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 2.7 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38	40	42	MHz
		V_{CC} = 2.7 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	37.6	40	42.4	MHz
		V_{CC} = 2.2 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(3)	34	40	46	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4)	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864		MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

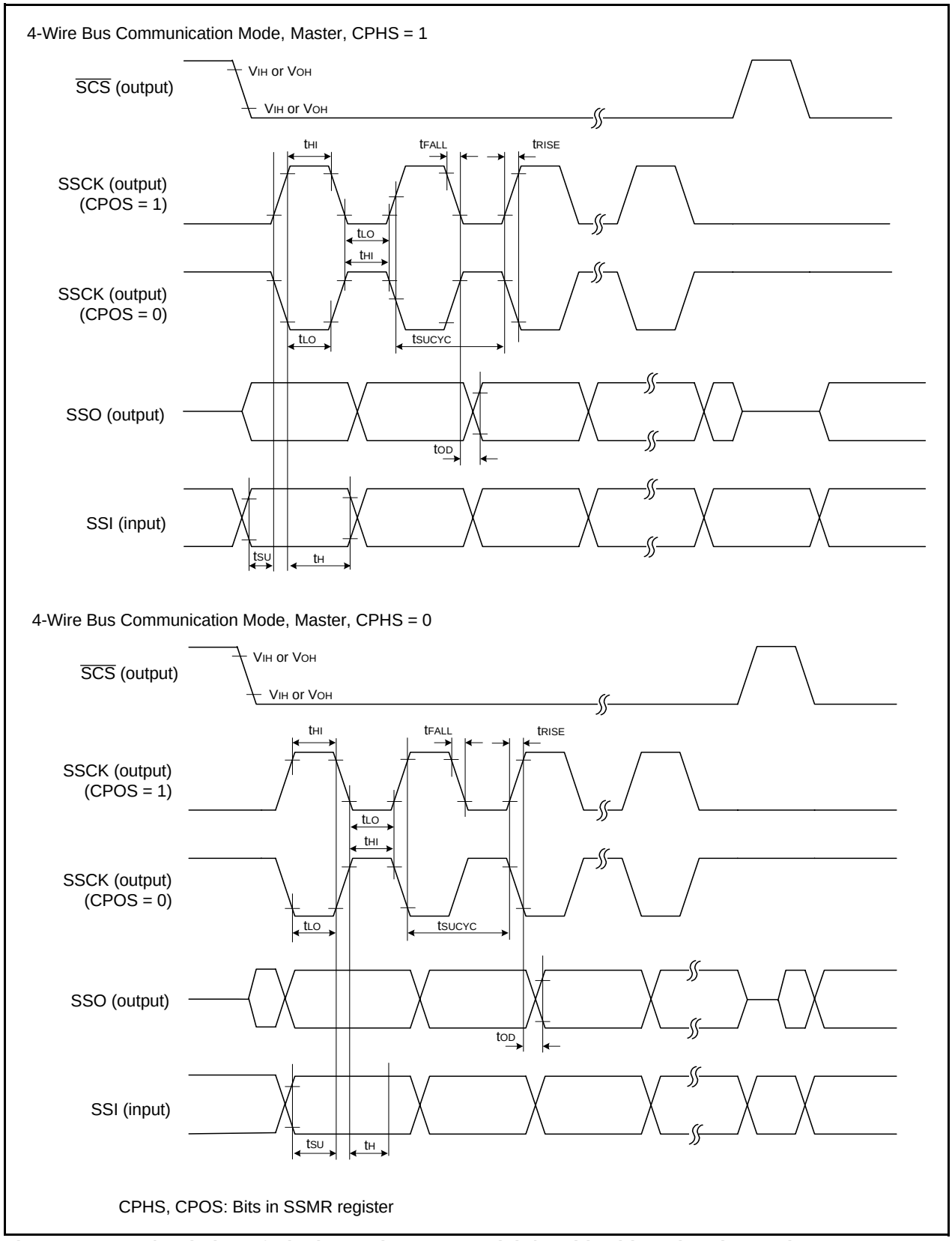


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

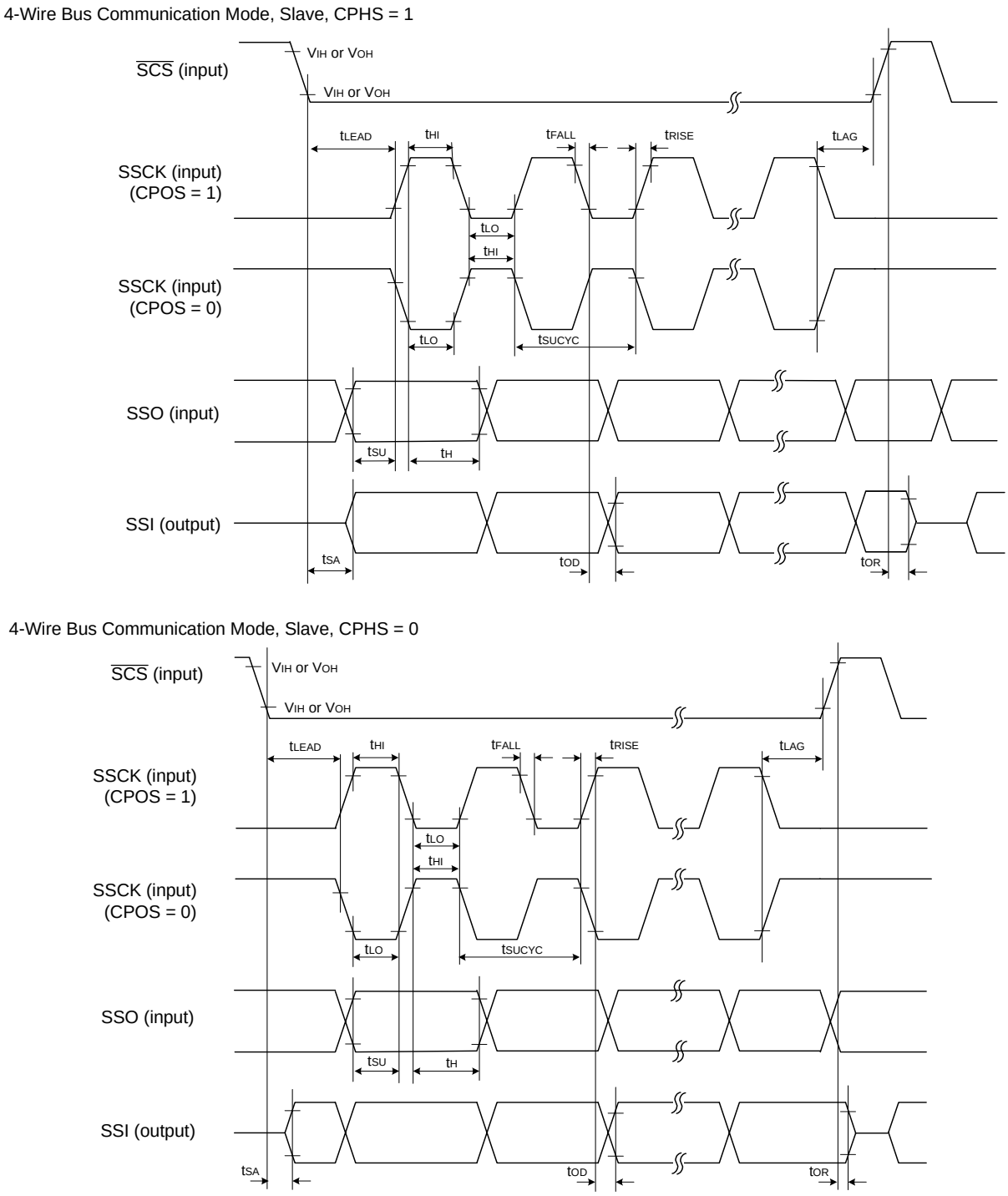


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

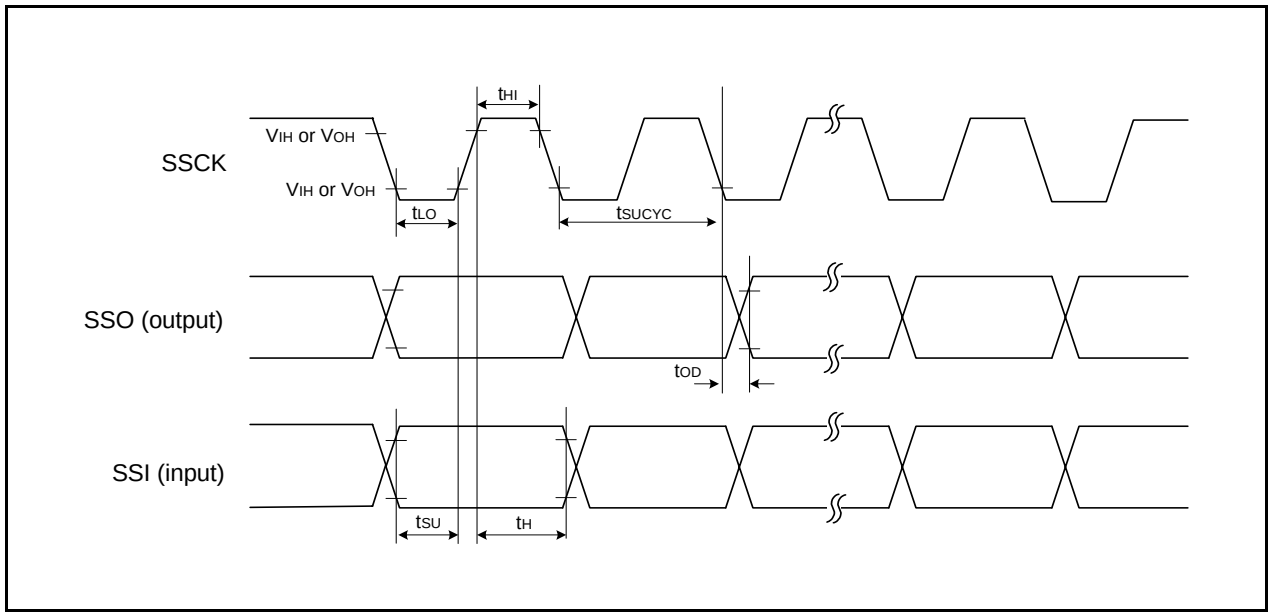


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.14 Timing Requirements of I²C bus Interface(1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$(2)	–	–	ns
t_{sf}	SCL, SDA input fall time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 20$(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$

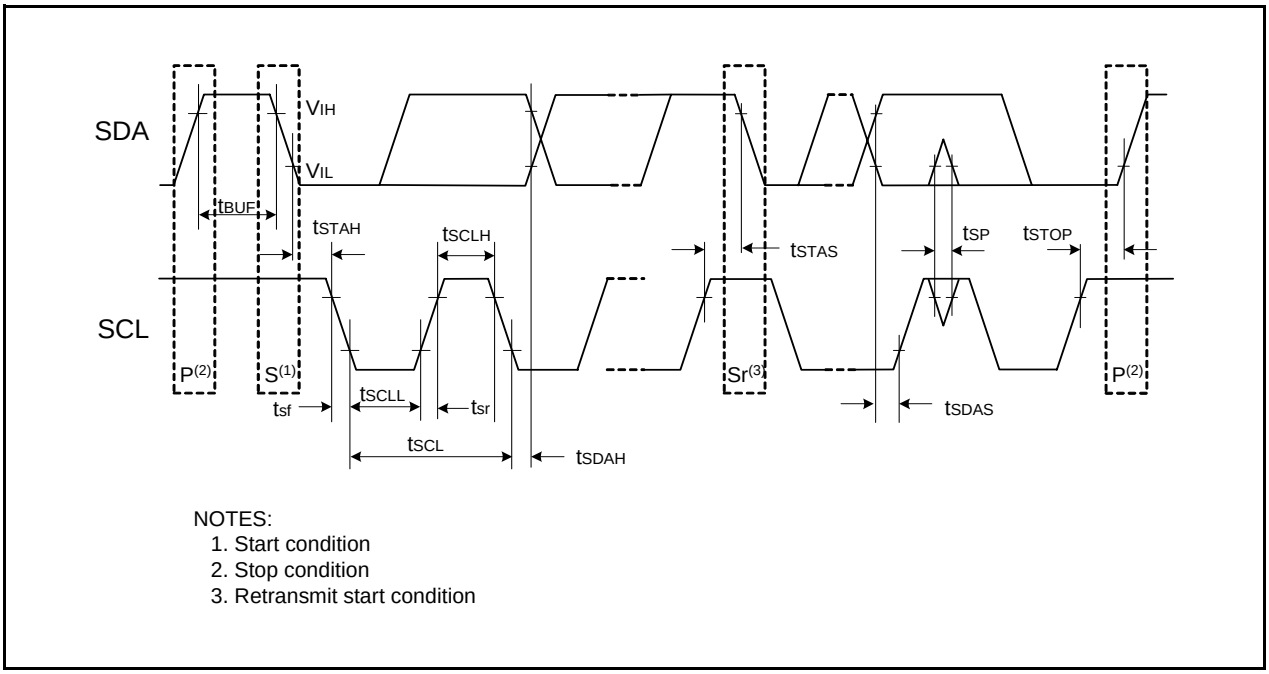


Figure 5.7 I/O Timing of I²C bus Interface

Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200 µA		V_{CC} – 0.5	–	V_{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 µA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 µA		–	–	0.45	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 µA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, KI2, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, Vcc = 5V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 5V		–	–	-5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 5V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.16 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA

Table 5.17 Electrical Characteristics (3) [Vcc = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V_{SS}	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.2	–	µA
		Increase during A/D converter operation	Without sample & hold	–	2.6	–	mA
			With sample & hold	–	1.6	–	mA
		Stop mode	XIN clock off, T_{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	µA
			XIN clock off, T_{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	µA

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.18 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

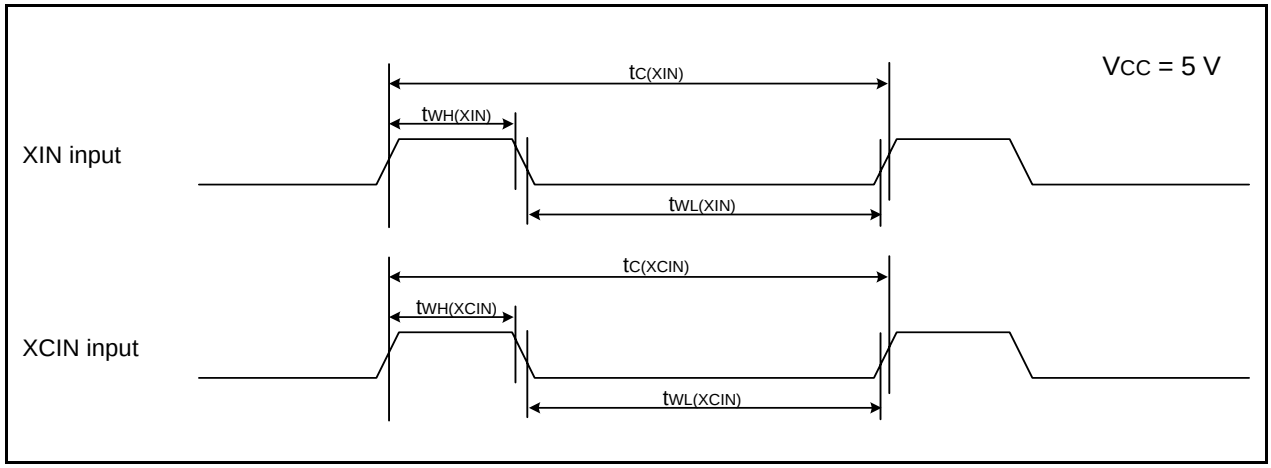


Figure 5.8 XIN Input and XCIN Input Timing Diagram when Vcc = 5 V

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

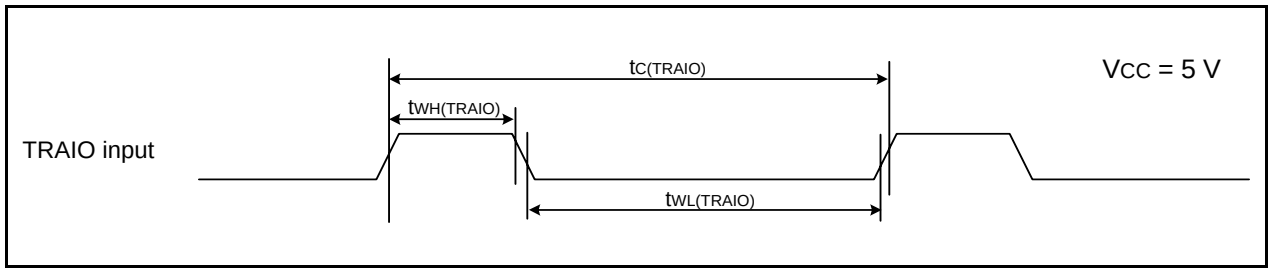


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

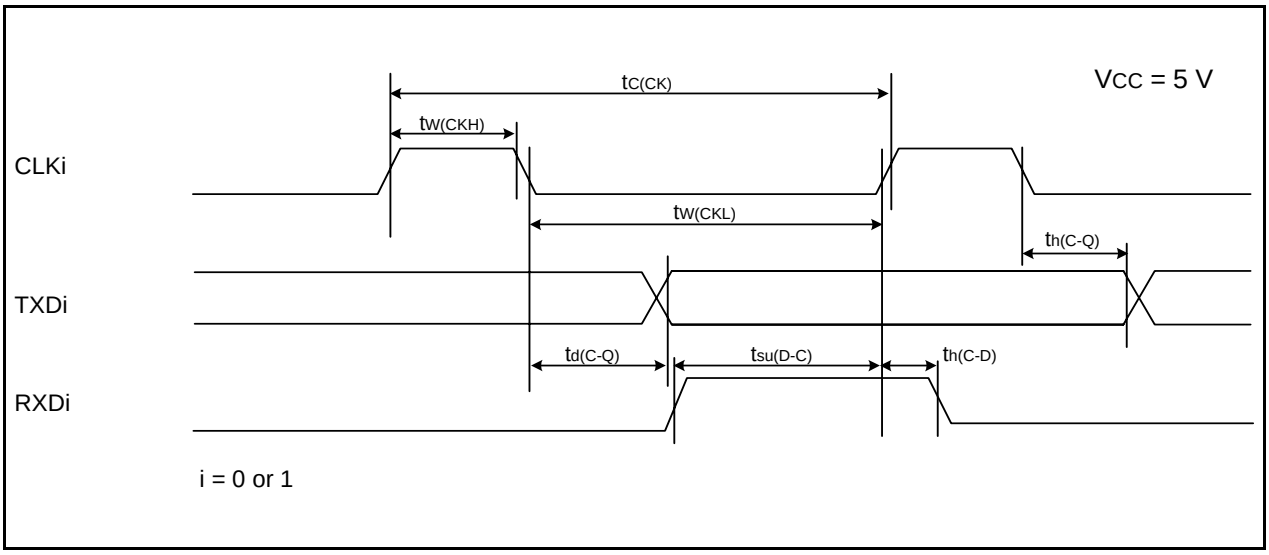


Figure 5.10 Serial Interface Timing Diagram when VCC = 5 V

Table 5.21 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

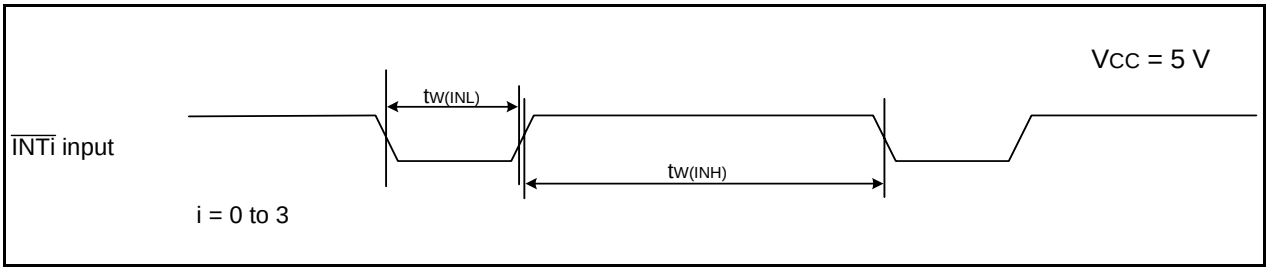


Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Table 5.22 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -1 mA		Vcc - 0.5	–	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -5 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -1 mA	Vcc - 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -50 µA	Vcc - 0.5	–	Vcc	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 5 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, Vcc = 3V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 3V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 3V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc =2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.23 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.8	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.0	–	µA
		Increase during A/D converter operation	Without sample & hold	–	0.9	–	mA
			With sample & hold	–	0.5	–	mA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at Topr = 25°C) [V_{CC} = 3 V]

Table 5.24 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

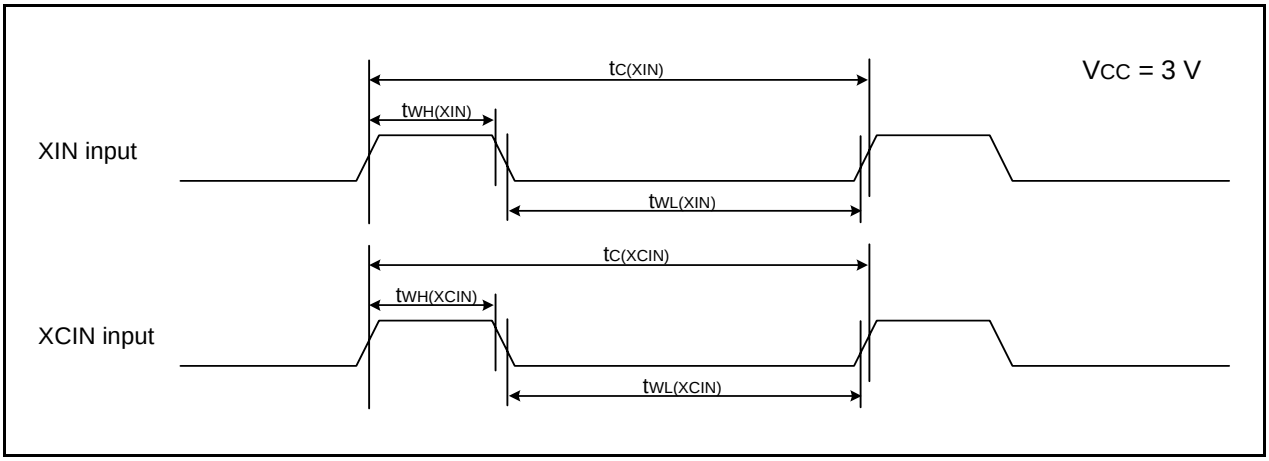


Figure 5.12 XIN Input and XCIN Input Timing Diagram when V_{CC} = 3 V

Table 5.25 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

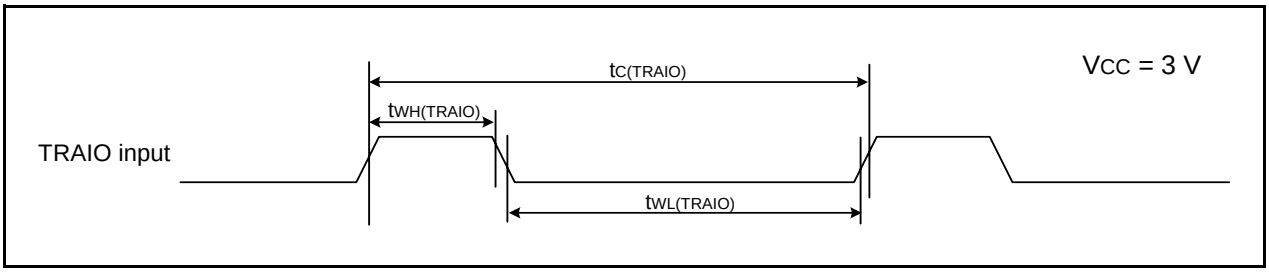


Figure 5.13 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

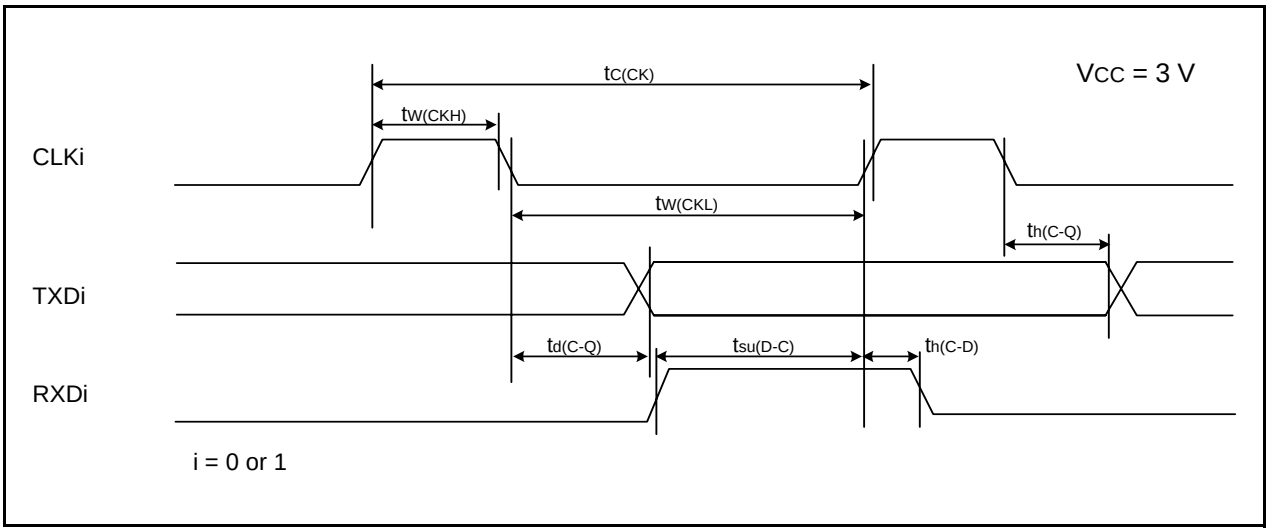


Figure 5.14 Serial Interface Timing Diagram when VCC = 3 V

Table 5.27 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

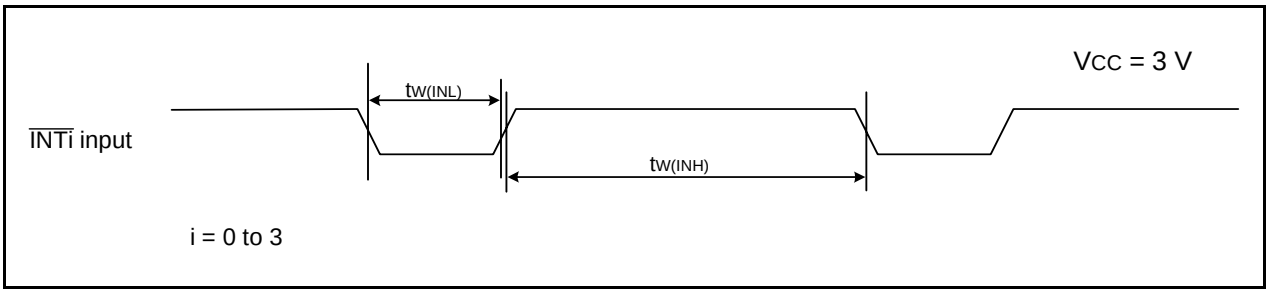


Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V

Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -1 mA		Vcc - 0.5	–	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -2 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -1 mA	Vcc - 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -50 µA	Vcc - 0.5	–	Vcc	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.05	0.3	–	V
		$\overline{RESET}$			0.05	0.15	–	V
I_{IH}	Input “H” current		VI = 2.2 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		100	200	600	kΩ
R_{fXIN}	Feedback resistance	XIN			–	5	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	35	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	100	230	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	25	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	1.8	–	µA
		Increase during A/D converter operation	Without sample & hold	–	0.4	–	mA
			With sample & hold	–	0.3	–	mA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V at Topr = 25°C) [V_{CC} = 2.2 V]

Table 5.30 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

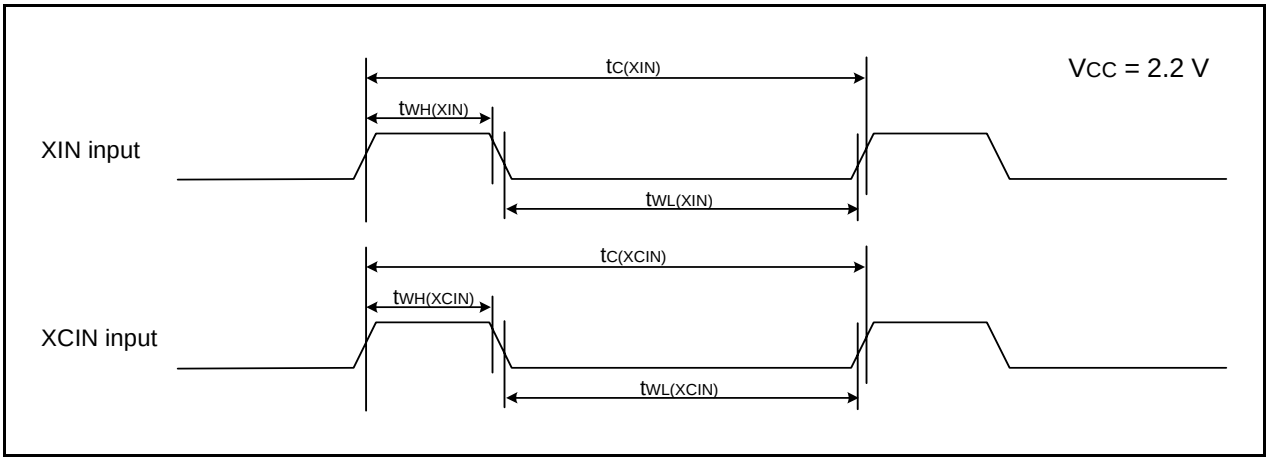


Figure 5.16 XIN Input and XCIN Input Timing Diagram when V_{CC} = 2.2 V

Table 5.31 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

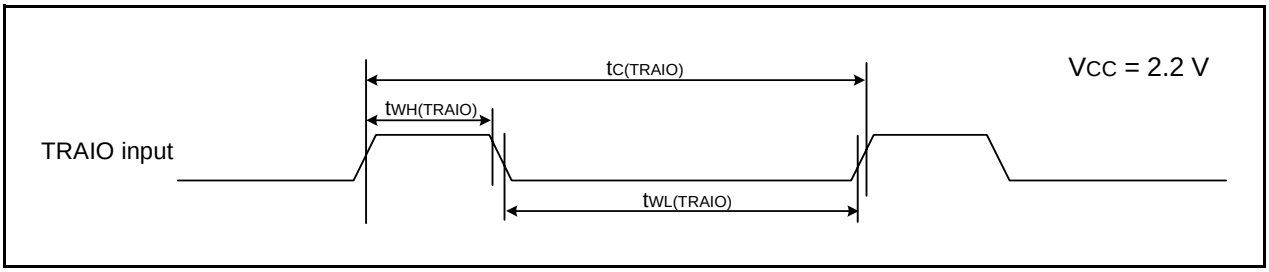


Figure 5.17 TRAIO Input Timing Diagram when V_{CC} = 2.2 V

Table 5.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

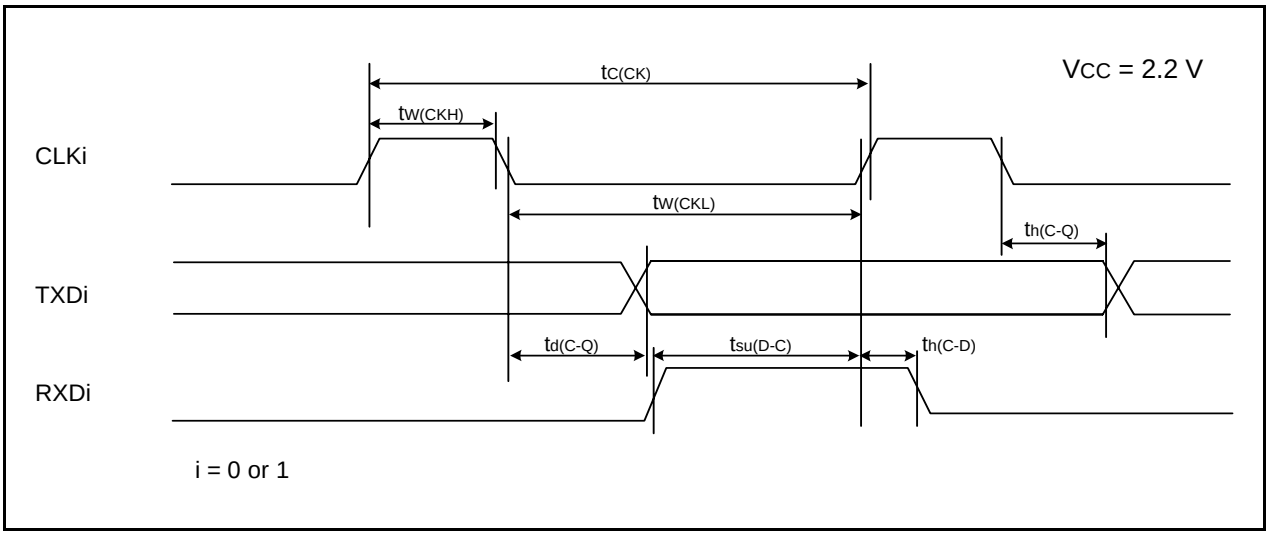


Figure 5.18 Serial Interface Timing Diagram when VCC = 2.2 V

Table 5.33 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	1000(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	1000(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

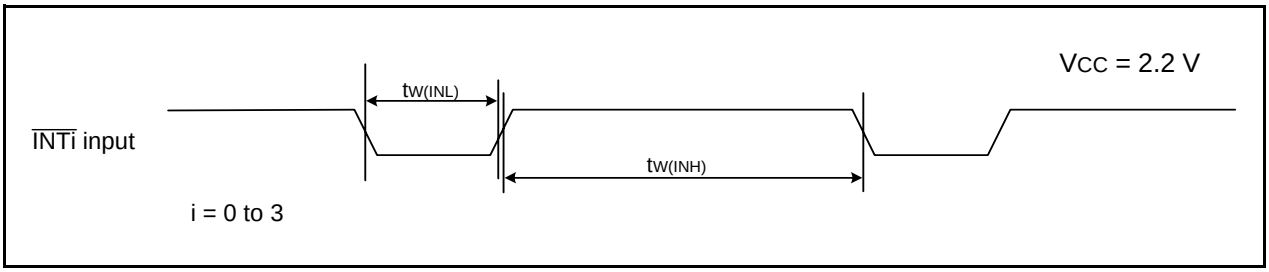


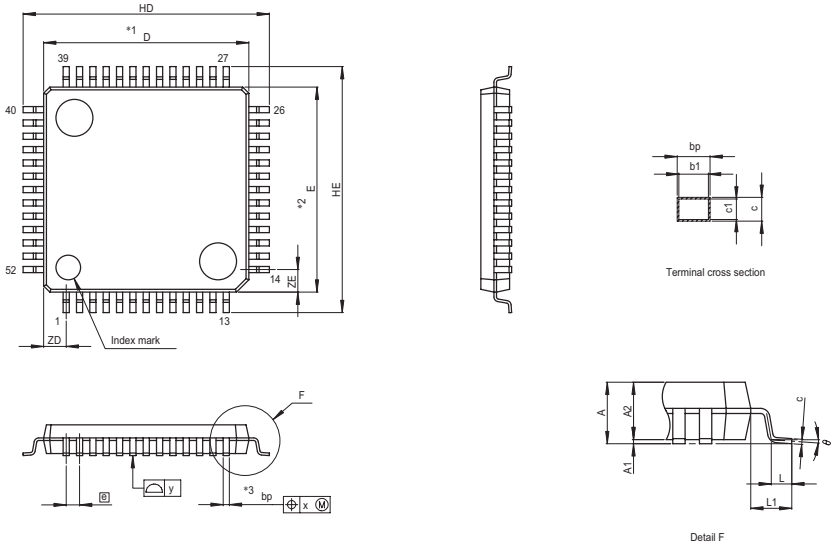
Figure 5.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g

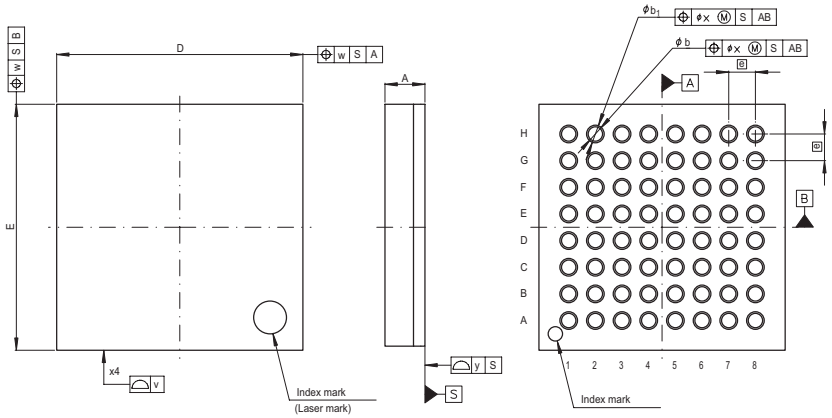
Under development



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Sep 17, 2004	-	First Edition issued
0.02	Dec 10, 2004	All pages	Part Number revised. R8C/26 → R8C/24, R8C/27 → R8C/25
		2, 3	Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance - Serial Interface: I^2C Bus Interface and Chip-select clock synchronous (SSU) added. - LIN Module added. - Interrupt: Internal factors revised; 10 → 11 - Note on Operating Ambient Temperature added.
		4	Figure 1.1 Block Diagram - LIN Module added. - Chip-select clock synchronous (SSU) is added to I^2C Bus Interface.
		5, 6	Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group Date and Development state revised.
		7	Figure 1.4 Pin Assignment P3_5/SCL → P3_5/SCL/SSCK, P3_3 → P3_3/SSI, P3_4/SDA → P3_4/SDA/SCS, P3_7 → P3_7/SSO, VSS/AVSS → VSS, XIN/P4_6 → P4_6/XIN, VCC/AVSS → VCC 12pin P1_7/TRAIO/INT1 to 22pin P1_0/KI0/AN8 → 20pin P1_7/TRAIO/INT1 to 30pin P1_0/KI0/AN8
		8	Table 1.5 Pin Description - Analog Power Supply Input eliminated. - SSU added.
		9	Table 1.6 Pin Name Information by Pin Number added.
		15	Table 4.1 SFR Information (1) - 0031h: Voltage Detection Register 1 → Voltage Detection A Register 1 - 0032h: Voltage Detection Register 1 → Voltage Detection A Register 2 01000001b → 00100001b (Note 4) - 0036h: "(3), 01000001b (4)" eliminated. - 0038h: Voltage Monitor 0 Control Register (2), VW0C, 00001000b (3), 01000001b (4) added.
		16	Table 4.2 SFR Information (2) - 0048h: Timer RD0 Interrupt Control Register, RD0IC, XXXXX000b added. - 0049h: Timer RD Interrupt Control Register, RDIC → Timer RD1 Interrupt Control Register, RD1IC - 004Fh: IIC Interrupt Control Register, IIC → IIC/SSU Interrupt Control Register, IIC2IC
		19	Table 4.5 SFR Information (3) - 0106h: LIN Control Register, LINCR, 00h added. -0107h: LIN Status Register, LINST, 00h added.

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Feb 24, 2005	1 to 3 5, 6	Pin type changed: 48-pin(under consideration) → 52-pin.
		5 to 7	Package type revised: 48-pin LQFP(under consideration) → PLQP0052JA-A
		8	Table 1.5 TCLK added, VREF revised.
		9	Table 1.6 revised.
		13, 14	Figures 3.1 and 3.2 part number revised.
		15	Tabel 4.1 revised: - 000Fh: 000XXXXXb → 00011111b - 0023h: FR0 → FRA0 - 0024h: FR1 → FRA1 - 0025h: FR2 → FRA2 - 0031h: Voltage Detection A Register 1, VC1 → Voltage Detection Register 1, VCA1 - 0032h: Voltage Detection A Register 2, VC2 → Voltage Detection Register 2, VCA2
		17	Tabel 4.3 Register name and the value after reset at 00B8h to 00BFh revised; NOTE2 added.
		19	Tabel 4.5 revised: - 0107h: LINSR → LINST - 0137h to 013Fh: Register symbol revised
		20	Tabel 4.6 revised: - 0140h to 015Fh: Register symbol revised - 0158h, 0159h: Timer RD General Register → Timer RD General Register A1
0.20	Mar 8, 2005	2, 3 8	Tables 1.1, 1.2 and 1.5 revised: “main clock” → “XIN clock”; “sub clock” → “XCIN clock”
		15	- 0023h to 0025h: 40MHz On-Chip Oscillator Control Register → High-Speed On-Chip Oscillator Control Register
0.30	Sep 01, 2005	2, 3	Table 1.1 R8C/24 Group Performance, Table 1.2 R8C/25 Group Performance • Serial Interface revised: - Serial Interface: 2 channels Clock synchronous serial I/O, UART - Clock Synchronous Serial Interface: 1 channel I^2C bus Interface(1), Clock synchronous serial I/O with chip select
		4	Figure 1.1 Block Diagram • UART or Clock Synchronous Serial Interface: “(8 bits × 1 channel)” → “(8 bits × 2 channels)” revised • UART (8 bits × 1 channel) deleted
		5, 6	Table 1.3 Product Information of R8C/24 Group, Table 1.4 Product Information of R8C/25 Group “Flash Memory Version” → “N Version” revised

Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	7	Figure 1.4 Pin Assignment • Pin name revised; VSS → VSS/AVSS, VCC → VCC/AVCC, P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$) → P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2), P6_6/$\overline{\text{INT2}}$/(TXD1) → P6_6/$\overline{\text{INT2}}$/TXD1, P6_7/$\overline{\text{INT3}}$/(RXD1) → P6_7/$\overline{\text{INT3}}$/RXD1, P6_5 → P6_5/CLK1 • NOTE2 added
		8	Table 1.5 Pin Description • Analog Power Supply Input: line added • $\overline{\text{INT}}$ Interrupt Input: "$\overline{\text{INT0}}$ Timer RD input pins. $\overline{\text{INT1}}$ Timer RA input pins." added • Serial Interface: "CLK1" added • "I2C Bus Interface (IIC)" → "I2C Bus Interface" • "SSU" → "Clock Synchronous Serial I/O with Chip Select"
		9	Table 1.6 Pin Name Information by Pin Number revised • Pin Number 10: "VSS" → "VSS/AVSS" • Pin Number 12: "$\overline{\text{VCC}}$" → "VCC/AVCC" • Pin Number 27: "$\overline{\text{INT0}}$" added • Pin Number 28: "(TXD1)" → "TXD1" • Pin Number 29: "(RXD1)" → "RXD1" • Pin Number 35: "CLK1" added
		15	Tabel 4.1 SFR Information(1) revised: • 0012h: X0h → 00h • 0013h: XXXXXX00b → 00h • 0016h: X0h → 00h • 0036h: Voltage Monitor 1 Control Register(2) → Voltage Monitor 1 Control Register(5) • 0038h: 00001000b(3), 01000001b(4) → 0000X000b(3), 0100X001b(4) • NOTES2, 5: "the voltage monitor 1 reset" added • NOTE3: "voltage monitor 1 reset" → "voltage monitor 0 reset"
		16	Tabel 4.2 SFR Information(2) revised: • 0048h: RD0IC → TRD0IC • 0049h: RD1IC → TRD1IC • 004Ah: REIC → TREIC • 004Fh: SSU/IIC Interrupt Control Register, IIC2AIC → SSU/IIC Interrupt Control Register(2), SSUAIC/IIC2AIC • 0056h: RAIC → TRAIC • 0058h: RBIC → TRBIC • NOTE2 added
		17	Tabel 4.3 SFR Information(3) revised: • 00BCh: 00h → 00h/0000X000b
		18	Tabel 4.4 SFR Information(4) revised: • 00D6h: 00000XXXb → 00h • 00F5h: UART1 Function Select Register, U1SR, XXh added

Rev.	Date	Description	
		Page	Summary
0.30	Sep 01, 2005	19	Tabel 4.5 SFR Information(5) revised: • 0118h : Timer RE Second Data Register/Counter Register → Timer RE Second Data Register/Counter Data Register
		20	Tabel 4.6 SFR Information(6) revised: • 0145h POCR0 → TRDPOCR0 • 0146h, 0147h TRDCNT0 → TRD0 • 0148h, 0149h GRA0 → TRDGRA0 • 014Ah, 014Bh GRB0 → TRDGRB0 • 014Ch, 014Dh GRC0 → TRDGRC0 • 014Eh, 014Fh GRD0 → TRDGRD0 • 0155h POCR1 → TRDPOCR1 • 0156h, 0157h TRDCNT1 → TRD1 • 0158h, 0159h GRA1 → TRDGRA1 • 015Ah, 015Bh GRB1 → TRDGRB1 • 015Ch, 015Dh GRC1 → TRDGRC1 • 015Eh, 015Fh GRD1 → TRDGRD1
		21	Tabel 4.7 SFR Information(7) revised: • 01B5h: 01000101b → 1000000Xb • 01B7h: XX000001b → 00000001b • FFFFh: (Note 2) added
		22 to 44	5. Electrical Characteristics added
0.40	Jan 24, 2006	all pages	• “Preliminary” deleted • Symbol name “TRDMDR” → “TRDMR”, “SSUAIC” → “SSUIC”, and “IIC2AIC” → “IICIC” revised • Pin name “TCLK” → “TRDCLK” revised
		2	Table 1.1 Functions and Specifications for R8C/24 Group revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; “Peripheral Functions” added, “System Clock Generation” → “System Clock Generator” revised
		5	Table 1.3 Product Information for R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group revised
		7	Figure 1.4 Pin Assignments (Top View) “TCLK” → “TRDCLK” revised
		8	Table 1.5 Pin Functions “TCLK” → “TRDCLK” revised
		9	Table 1.6 Pin Name Information by Pin Number; “TCLK” → “TRDCLK” revised
		10	Figure 2.1 CPU Registers; “Reserved Area” → “Reserved Bit” revised
		12	2.8.10 Reserved Area; “Reserved Area” → “Reserved bit” revised
		13	Figure 3.1 Memory Map of R8C/24 Group; “Program area” → “program ROM” revised
		14	3.2 R8C/25 Group, Figure 3.2 Memory Map of R8C/25 Group; “Data area” → “data flash”, “Program area” → “program ROM” revised

Rev.	Date	Description	
		Page	Summary
0.40	Jan 24, 2006	15	Table 4.1 SFR Information(1); 0024h: "TBD" → "When shipping" NOTES 3 and 4 revised
		19	Table 4.5 SFR Information (5); 0118h: "Timer RE Second Data Register" → "Timer RE Second Data Register / Counter Data Register" 0119h: "Timer RE Minute Data Register" → "Timer RE Minute Data Register / Compare Data Register" 0138h: "TRDMDR" → "TRDMR" 013Bh: "Timer RD Output Master Enable Register" → "Timer RD Output Master Enable Register 1"
		22	Table 5.1 Absolute Maximum Ratings; "VCC" → "VCC/AVCC" revised Table 5.2 Recommended Operating Conditions revised
		23	Table 5.3 A/D Converter Characteristics revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics revised
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical revised
		26	Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics revised Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics revised Table 5.8 Voltage Detection 2 Circuit Electrical Characteristics revised
		28	Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.13 Power Supply Circuit Timing Characteristics revised
		29	Table 5.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select revised
		33	Table 5.15 Timing Requirements of I^2C bus Interface NOTE1 revised
		34	Table 5.16 Electrical Characteristics (1) [VCC = 5 V] revised
		35	Table 5.17 Electrical Characteristics (2) [VCC = 5 V] revised
		36	Table 5.18 XIN Input, XCIN Input revised
		37	Table 5.20 Serial Interface revised
		38	Table 5.22 Electrical Characteristics (3) [VCC = 3 V] revised
		39	Table 5.23 Electrical Characteristics (4) [Vcc = 3 V] revised
		40	Table 5.24 XIN Input, XCIN Input revised
		41	Table 5.26 Serial Interface revised
		42	Table 5.28 Electrical Characteristics (5) [VCC = 2.2 V] revised
		43	Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		44	Table 5.30 XIN Input, XCIN Input revised Table 5.31 TRAIO Input, $\overline{INT1}$ Input revised
		45	Table 5.32 Serial Interface revised Table 5.33 External Interrupt $\overline{INTi}$ (i = 0, 2, 3) Input

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.40	Jan 24, 2006	46	Package Dimensions; "TBD" → "PLQP0052JA-A (52P6A-A)" added
1.00	May 31, 2006	all pages	"Under development" deleted
		1	1. Overview; "data flash ROM" → "data flash" revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; "System clock generator" → "System clock generation circuit" revised
		5 to 6	Table 1.3 Product Information for R8C/24 Group and Table 1.4 Product Information for R8C/25 Group; A part of (D) mark is deleted.
		9	Table 1.6 Pin Name Information by Pin Number NOTE1 added
		15	Table 4.1 SFR Information(1); 001Ch: "00h" → "00h, 10000000b" revised 0029h: High-Speed On-Chip Oscillator Control Register 4 FRA4 When shipping added 002Bh: High-Speed On-Chip Oscillator Control Register 6 FRA6 When shipping added NOTE6 added
		19	Table 4.5 SFR Information(5); 0118h: Timer RE Second Data Register / Counter Data Register, 0119h: Timer RE Minute Data Register / Compare Data Register register name revised
		20	Table 4.6 SFR Information(6); 0143h: "11000000b" → "11100000b" revised
		22	Table 5.2 Recommended Operating Conditions revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics revised
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics revised
		26	Figure 5.2 Time delay until Suspend title revised
		27	Table 5.9 Voltage Monitor 0 Reset Electrical Characteristics → Table 5.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics revised Table 5.10 Power-on Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 0 Reset) deleted Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised
		28	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 5.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised
		35	Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] revised
		39	Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] revised
		43	Table 5.28 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		46	Package Dimensions; "The latest package ... Renesas Technology website." added

REVISION HISTORY	R8C/24 Group, R8C/25 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jul 14, 2006	all pages	“PTLG0064JA-A (64F0G)” package added
		1	1. Overview; “... or a 64-pin molded-plastic FLGA.“ added
		2, 3	Table 1.1 Functions and Specifications for R8C/24 Group, Table 1.2 Functions and Specifications for R8C/25 Group; Package: “64-pin molded-plastic FLGA” added
		5	Table 1.3 Product Information for R8C/24 Group, Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group revised
		6	Table 1.4 Product Information for R8C/25 Group, Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group revised
		7	Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View); NOTE3 revised
		8	Figure 1.5 PTLG0064JA-A Package Pin Assignments added
		14	Figure 3.1 Memory Map of R8C/24 Group revised
		15	Figure 3.2 Memory Map of R8C/25 Group revised
		23	Table 5.1 Absolute Maximum Ratings; NOTE1 added
		47	Package Dimensions; “PTLG0064JA-A (64F0G)” added
3.00	Feb 29, 2008	all pages	Y version added Factory programming product added
		2, 3	Table 1.1, Table 1.2 Clock; “Real-time clock (timer RE)” added
		5, 7	Table 1.3, Table 1.4 revised
		6, 8	Figure 1.2, Figure 1.3; ROM number “XXX” added
		16, 17	Figure 3.1, Figure 3.2; “Expanded area” deleted
		18	Table 4.1 revised
		26	Table 5.2 NOTE2 revised
		32	Table 5.10; revised, NOTE4 added Table 5.11; Oscillation stability time: Condition “V_{CC} = 5.0 V, Topr = 25°C” deleted
		38	Table 5.15; I_{IH}, I_{IL}, R_{PULLUP} Condition: “Vcc = 5V” added
		39	Table 5.16; Condition: High-speed on-chip oscillator mode revised
		40	Table 5.17 added
		41	Figure 5.8 revised
		43	Table 5.22; I_{IH}, I_{IL}, R_{PULLUP} Condition: “Vcc = 3V” added
		44	Table 5.23; Condition “Increase during A/D converter operation” added
		45	Figure 5.12 revised
		48	Table 5.29; Condition “Increase during A/D converter operation” added
		49	Figure 5.16 revised

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