

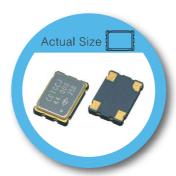
OC Type

7.0 x 5.0 mm SMD Crystal Oscillator

- Typical $7.0 \times 5.0 \times 1.3$ mm ceramic SMD package.
- Output frequency up to 166MHz
- Tr-state enable/disable.

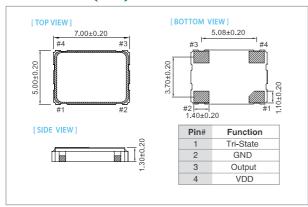
TYPICAL APPLICATION

- xDSL, WLAN, Fiber/10G-Bit Ethernet
- Notebook, PDA
- PC main board, VGA card

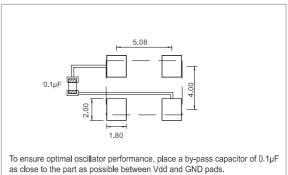


RoHS Compliant

DIMENSION (mm)



SOLDER PAD LAYOUT (mm)



ELECTRICAL SPECIFICATION

Parameter	3.3V		2.5V		1.8V		unit
	Min.	Max.	Min.	Max.	Min.	Max.	uriit
Supply Voltage Variation(VDD)	VDD-10%	VDD+10%	VDD-10%	V DD+10%	VDD-10%	VDD+10%	V
Frequency Range	0.0137	166	0.0137	133	0.0137	125	MHz
Standard Frequency	2.048, 25, 26, 27, 50, 66, 667, 100, 125						
Supply Current							
13.7 kHz ≦ Fo ≦ 70 kHz	_	1	_	1	_	1	
$0.3125 \text{ MHz} \leq \text{Fo} < 35.328 \text{ MHz} (A1)$	_	10	_	8	_	7	
30 MHz ≦ Fo < 75 MHz	_	20	_	18	_	15	mA
75 MHz ≦ Fo < 133 MHz	_	35	_	30	_	25	
133 MHz ≦ Fo	_	45	_	40	_	_	
Output Level (CMOS) Output High (Logic "1")	2.97	-	2.25	_	1.62	_	V
Output Low (Logic "0")	_	0.33	_	0.25	_	0.18	\ \ \
Transition Time:Rise/Fall Time							
13.7 kHz ≤ Fo ≤ 70 kHz	-	50	_	50	_	50	
0.3125 MHz ≦ Fo < 100 MHz	_	5	_	5	_	5	nSec
100 MHz ≦ Fo	_	3	_	3	_	3	
Start Time	-	5	_	5	_	5	mSec
Output Drive Capability (CL)	-	15	_	15	_	15	рF
Tri-State (Input to Pin1) Enable (High voltage or floating)	2.31	_	1.75	_	1.26	_	V
Disable (Low voltage or GND)	-	0.99	_	0.75	_	0.54	V
Period Jitter(Pk-Pk)	_	40	_	40	_	40	pSec
RMS Phase Jitter (Integrated 12 kHz~20 MHz)	-	1	_	1	_	1	pSec
Standby Current	_	10	_	10		10	μΑ
Aging (@ 25°C 1st year)	-	±3	_	±3	_	±3	ppm
Storage Temp. Range	-55	125	-55	125	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C)	±20	±25	±50
-10 ~ +60	0	0	0
-20 ~ +70	Δ	0	0
-40 ~ +85	\triangle	0	0
-40 ~ +125	×	×	0

^{* ○:} Available △:Conditional X: Not available

Note: not all combination of options are available. Other specifications may be available upon request.

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⁺ Transition times are measured between 10% and 90% of VDD, with an output load of 15pF.

^{*} Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration