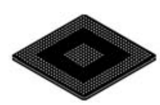
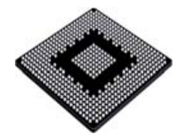
Freescale Semiconductor
Data Sheet: Advance Information

Document Number: MPC5676R
Rev. 4, 16 Feb 2016

MPC5676R



TEPBGA–416
27 mm x 27 mm



TEPBGA–516
27mm x 27mm

MPC5676R Microcontroller Data Sheet

On-chip modules available within the family include the following features:

- Two identical dual issue, 32-bit CPU core complexes (e200z7), each with
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  - Signal processing extension (SPE) instruction support for digital signal processing (DSP)
  - Single-precision floating point operations (FPU)
  - 16 KB I-Cache and 16 KB D-Cache
  - Hardware cache coherency between cores
- 16 Hardware semaphores
- 3 channel CRC module
- 6MB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 384KB on-chip general-purpose SRAM including 48KB of standby RAM
- Two multi-channel direct memory access controllers (eDMA)
  - 64 channels per eDMA
- Dual core Interrupt controller (INTC)
- Phase-locked loop with FM modulation (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- External Bus Interface (EBI) for calibration and application development
- System integration unit (SIU) with error correction status module (ECSM)
- Four protected port output pins (PPO)
- Boot assist module (BAM) supports serial bootload via CAN or SCI
- Three second-generation enhanced time processor units (eTPU2)
  - Up to 96 eTPU2 channels (32 channels per eTPU2)
  - total of 36 KB code RAM
  - total of 9 KB parameter RAM
- Enhanced modular input output system supporting 32 unified channels (eMIOS) with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two enhanced queued analog-to-digital converter (eQADC) modules with
  - two separate analog converters per eQADC module
  - support for a total of 64 analog input pins, expandable to 176 inputs with off-chip multiplexers
  - one absolute reference ADC channel
  - interface to twelve hardware decimation filters
  - enhanced 'Tap' command to route any conversion to two separate decimation filters
  - Temperature sensor
- Five deserial serial peripheral interface (DSPI) modules
- Three enhanced serial communication interface (eSCI) modules
- Four controller area network (FlexCAN) modules
- Dual-channel FlexRay controller
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard.
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller regulates supply voltage down to 1.2 V for core logic
- Self Test capability

Table of Contents

1 Ordering Information

1.1 Orderable Parts

Figure 1 and Table 1describe and list the orderable part numbers for the MPC5676R.

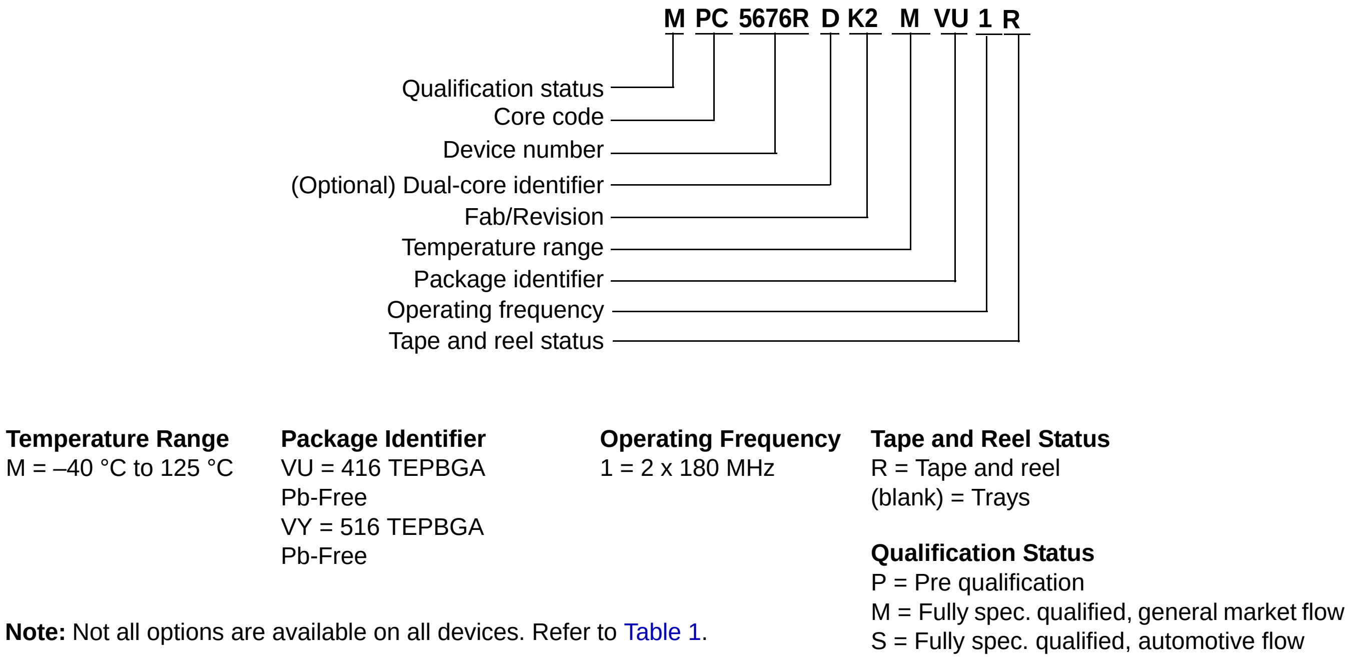


Figure 1. MPC5676R Orderable Part Number Description

Table 1. Orderable Part Numbers

NXP Part Number[1]	Package Description	Speed (MHz)[2]		Operating Temperature[3]	
		Nominal	Max[4] (f_{MAX})	Min (T_L)	Max (T_H)
SPC5676RDK2MVU1R	MPC5676R 416 package Lead-free (Pb-free)	180	184	–40 °C	125 °C
SPC5676RDK2MVY1R	MPC5676R 516 package Lead-free (Pb-free)	180	184	–40 °C	125 °C

1 All packaged devices are PPC5676R, rather than MPC5676R or SPC5676R, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.
Not all configurations are available in the PPC parts.

2 For the operating mode frequency of various blocks on the device, see Table 28.

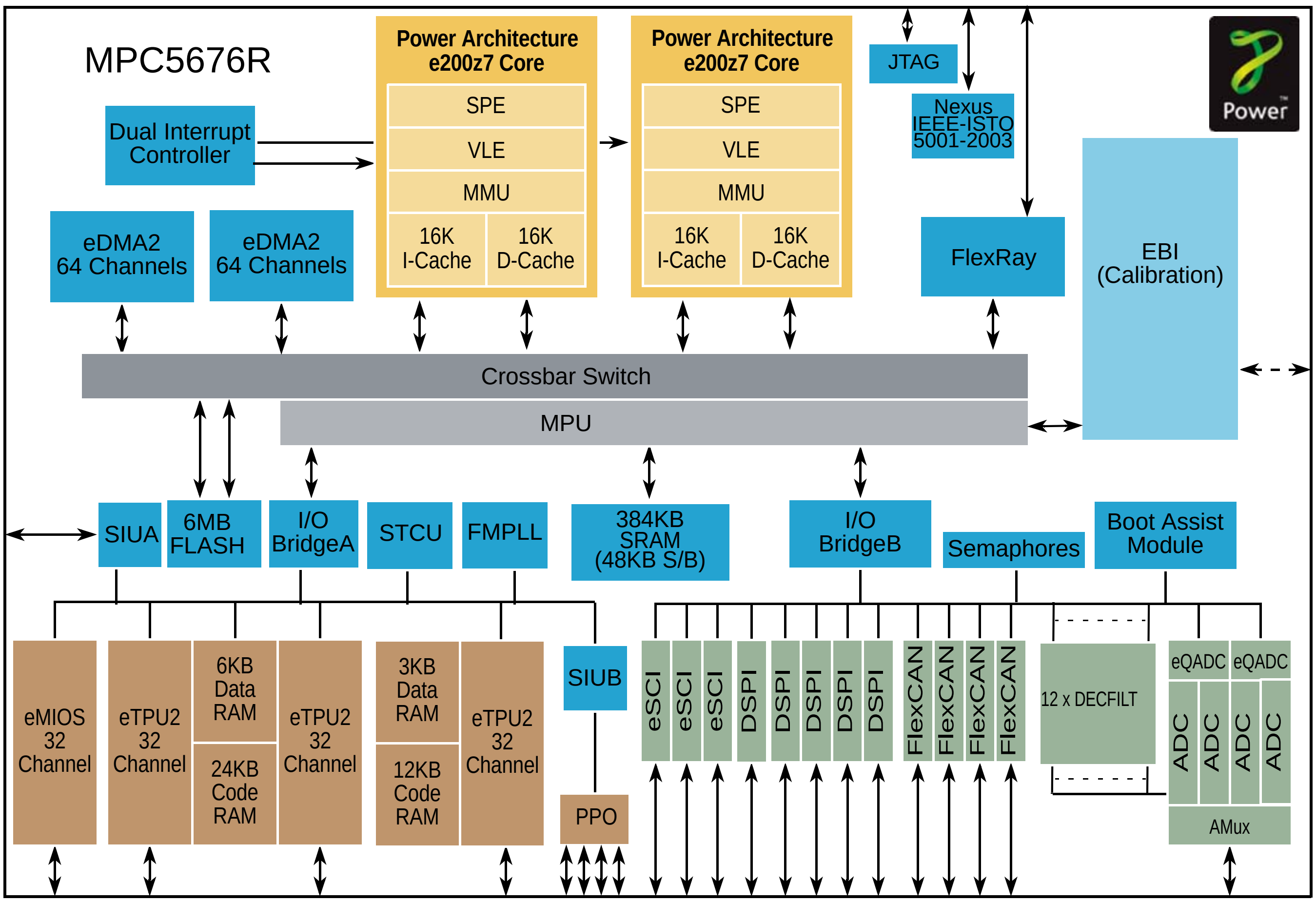
3 The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

4 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 180 MHz parts allow for 180 MHz system clock + 2% FM.

2 MPC5676R Blocks

2.1 Block Diagram

The following figure shows a top-level block diagram of the MPC5676R. The purpose of the block diagram is to show the general interconnection of functional modules through the crossbar switch and from the Dual Interrupt Controller, and provide an indication of the modules that connect to external pins. For clarity, the following modules are omitted from the diagram: PMU, SWT, STM, PIT, ECSM, DTS, and CRC.



LEGEND

ADC – Analog to Digital Convertor
AMux – Analog Pin Multiplexer
D-Cache – Data Cache
DECFILT – Decimation Filter
DSPI – Deserial/Serial Peripheral Interface
EBI – External Bus Interface
eDMA2 – Enhanced Direct Memory Access controller version 2
eMIOS – Enhanced Modular I/O System
eQADC – Enhanced Queued Analog to Digital Converter
eSCI – Enhanced Serial Communications Interface
eTPU2 – Enhanced Time Processing Unit version 2
FlexCAN – Flexible Controller Area Network controller
FMPLL – Frequency Modulated Phase Lock Loop clock generator
I-Cache – Instruction Cache
IRC – Internal RC Oscillator
JTAG – Joint Test Action Group controller
MMU – Memory Management Unit
MPU – Memory Protection Unit
PPO – Protected Port Output
S/B – Stand-by
SIUA – System Integration Unit A
SIUB – System Integration Unit B
SPE – Signal Processing Engine
SRAM – Static RAM
STCU – Self Test Control Unit
VLE – Variable Length instruction Encoding

Figure 2. MPC5676R Block Diagram

3 Pin Assignments

3.1 416-ball TEPBGA Pin Assignments

Figure 3 shows the 416-ball TEPBGA pin assignments.

CAUTION

This ball map is preliminary and subject to change. Do not use it for board design.

MPC5676R 416-ball TEPBGA

(as viewed from top through the package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VDD	RSTOUT	ANA0	ANA4	ANA8	ANA11	ANA15	VDDA_A0	REF-BYPCA1	VRL_A	VRH_A	AN28	AN32	AN36	VDDA_B0	REF-BYPCB1	VRL_B	VRH_B	ANB7	ANB11	ANB14	ANB17	ANB21	ANB23	VSS	A
B	VDDEH1	VSS	VDD	TEST	ANA1	ANA5	ANA10	ANA14	VDDA_A1	VSSA_A1	REF-BYPCA	AN24	AN27	AN29	AN33	VDDA_B1	VSSA_B0	REF-BYPCB	ANB6	ANB8	ANB10	ANB15	ANB18	ANB22	VSS	TCRCLKC	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2	ANA6	ANA9	ANA13	ANA17	ANA19	ANA21	ANA23	AN26	AN30	AN34	AN37	AN38	ANB0	ANB4	ANB5	ANB12	ANB16	ANB19	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3	ANA7	ANA12	ANA16	ANA18	ANA20	ANA22	AN25	AN31	AN35	AN39	ANB1	ANB2	ANB3	ANB9	ANB13	ANB20	VSS	VDDEH7	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26																			VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22																			ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA15	ETPUA16	ETPUA17	ETPUA18																			ETPUC11	ETPUC12	ETPUC13	ETPUC14	G
H	ETPUA11	ETPUA12	ETPUA14	ETPUA13																			ETPUC15	ETPUC16	ETPUC17	ETPUC18	H
J	ETPUA7	ETPUA8	ETPUA9	ETPUA10																			ETPUC19	ETPUC20	ETPUC21	ETPUC22	J
K	ETPUA3	ETPUA4	ETPUA5	ETPUA6						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC23	ETPUC24	ETPUC25	ETPUC26	K
L	TCRCLKA	ETPUA0	ETPUA1	ETPUA2						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC27	ETPUC28	ETPUC29	ETPUC30	L
M	VDD33_1	TXDA	RXDA	VSTBY						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						ETPUC31	ETPUB15	ETPUB14	VDDEH7	M
N	RXDB	BOOT-CFG1	WKPCFG	VDD						VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDEH6	ETPUB11	ETPUB12	ETPUB13	N
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V	MDO2	MDO3	MDO4	MDO5																			ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W	MDO6	MDO7	MDO8	VDDE2																			REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y	MDO9	MDO10	MDO11	MDO15																			ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA	MDO12	MDO13	MDO14	VDD33_2																			VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB	TDO	TCK	TMS	VDD																			VDD	ETPUB31	VSSFL	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	VSS	VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 3. MPC5676R 416-ball TEPBGA (full diagram)

3.2 516-ball TEPBGA Pin Assignments

Figure 4 shows the 516-ball TEPBGA pin assignments.

MPC5676R 516-ball TEPBGA

(as viewed from top through the package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A		VDD	RSTOUT	ANA0	ANA4	ANA9	ANA11	ANA15	VDDA_A0	REF–BYPCA1	VRL_A	VRH_A	AN28	AN29	AN36	VDDA_B0	REF–BYPCB1	VRL_B	VRH_B	ANB5	ANB9	ANB12	ANB18	ANB21	VSS		A
B	VDDEH1	VSS	VDD	TEST	ANA1	ANA5	ANA10	ANA14	VDDA_A1	VSSA_A1	REF–BYPCA	AN24	AN27	AN30	AN32	VDDA_B1	VSSA_B0	REF–BYPCB	ANB4	ANB8	ANB10	ANB13	ANB19	ANB22	VSS	VSS	B
C	ETPUA30	ETPUA31	VSS	VDD	ANA2	ANA6	ANA7	ANA13	ANA17	ANA19	ANA21	ANA22	AN25	AN31	AN34	AN39	AN37	ANB0	ANB7	ANB6	ANB11	ANB15	ANB20	VSS	ETPUC0	ETPUC1	C
D	ETPUA27	ETPUA28	ETPUA29	VSS	VDD	ANA3	ANA8	ANA12	ANA16	ANA18	ANA20	ANA23	AN26	AN33	AN35	AN38	ANB1	ANB2	ANB3	ANB14	ANB16	ANB17	VSS	VDDEH7	ETPUC2	ETPUC3	D
E	ETPUA23	ETPUA24	ETPUA25	ETPUA26	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ANB23	VSS	VSS	VDDEH7	ETPUC4	ETPUC5	ETPUC6	E
F	ETPUA19	ETPUA20	ETPUA21	ETPUA22	VSS	VDDE8		VDDE8		VDDE8	VDDE8		VSS	VSS		VDDE10	VDDE10		VDDE10		VDDE10	TCRCLKC	ETPUC7	ETPUC8	ETPUC9	ETPUC10	F
G	ETPUA11	ETPUA13	ETPUA15	ETPUA17	ETPUA18																	ETPUC11	ETPUC12	ETPUC13	ETPUC14	ETPUC15	G
H	ETPUA5	ETPUA7	ETPUA8	ETPUA3	ETPUA14	ETPUA16															ETPUC19	ETPUC16	ETPUC17	ETPUC18	ETPUC20	ETPUC21	H
J	ETPUA1	ETPUA2	ETPUA9	ETPUA4	ETPUA12																	ETPUC22	ETPUC23	ETPUC24	ETPUC26	ETPUC27	J
K	TXDB	TXDA	RXDA	TCRCLKA	ETPUA6	ETPUA10				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				ETPUC25	ETPUC28	ETPUC29	ETPUC30	ETPUC31	D_DAT15	K
L	PLLCFG1	PLLCFG2	BOOT–CFG1	BOOT–CFG0	RXDB	ETPUA0				VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VDD33_6	D_DAT14	D_DAT13	D_DAT12	D_DAT11	D_DAT10	L
M	VDD33_1	D_BDIP	PLLCFG0	VSTBY	WKPCFG					VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS					D_DAT9	D_DAT8	D_DAT7	D_DAT5	VDDEH7	M
N	D_WE0	D_WE2	D_WE3	VDD	RESET	VDDE8				VDDE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	D_DAT6	VDDEH6	D_DAT2	D_DAT3	D_DAT4	N
P	D_ADD9	D_ADD10	D_ADD11	VDDEH1	D_WE1	VDD33_1				VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS				VDDE10	ETPUB13	D_OE	D_ALE	D_DAT0	D_DAT1	P
R	D_ADD12	D_ADD13	D_ADD14	D_ADD15	D_ADD16					VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS	VSS					ETPUB9	ETPUB12	ETPUB14	ETPUB15	D_RD_WR	R
T	VDDE2	D_ADD18	D_ADD19	D_ADD20	D_ADD17	D_CS3				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB17	ETPUB3	ETPUB7	ETPUB8	ETPUB10	ETPUB11	T
U	D_CS2	JCOMP	RDY	MCKO	MSEO1	MSEO0				VDDE2	VDDE2	VDDE2	VSS	VSS	VSS	VSS	VSS				ETPUB23	ETPUB1	ETPUB2	ETPUB4	ETPUB5	ETPUB6	U
V	EVTI	EVTO	MDO0	MDO2	MDO3																	ETPUB21	ETPUB22	ETPUB16	TCRCLKB	ETPUB0	V
W	MDO4	MDO5	MDO6	VDDE2	MDO8	MDO1															ETPUB25	ETPUB29	REGSEL	ETPUB20	ETPUB19	ETPUB18	W
Y	MDO7	MDO9	MDO10	MDO11	MDO12																	ETPUB31	ETPUB26	ETPUB27	ETPUB24	REGCTL	Y
AA	MDO13	MDO14	MDO15	VDD33_1	VDDE8	VSS		PCSA5		SOUTB	VDD33_4		VDDE9	VDD33_4		EMIOS23	EMIOS31		CNRXB		VSS	VDDE10	VDD33_3	ETPUB28	VDDREG	VSSSYN	AA
AB	TDO	TCK	TMS	VDD	VSS	VDDE9	VDDE9	SCKA	SINB	D_CS1	D_ADD21	D_ADD29	EMIOS1	EMIOS11	EMIOS17	EMIOS19	EMIOS29	VDDE9	VDDE9	VDDE9	VDDE9	VSS	VDD	ETPUB30	VSSFL	EXTAL	AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	SOUTA	SCKB	PCSB3	VDDEH3	VDDEH4	VDD	EMIOS0	EMIOS8	EMIOS13	EMIOS22	EMIOS24	EMIOS28	CNTXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA0	PCSA3	PCSB2	D_CS0	D_ADD22	D_ADD25	D_ADD28	EMIOS2	EMIOS7	EMIOS12	EMIOS16	EMIOS18	EMIOS27	CNRXA	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSB5	SINA	PCSB1	D_TS	D_ADD23	D_ADD26	D_ADD30	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS21	EMIOS26	CNTXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF		VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSA2	PCSB4	PCSB0	D_TA	D_ADD24	D_ADD27	D_CLKOUT	EMIOS4	EMIOS5	EMIOS9	EMIOS20	EMIOS14	EMIOS25	EMIOS30	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5		AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 4. MPC5676R 516-ball TEPBGA (full diagram)

3.3 Pin Muxing and Reset States

See Appendix A, Signal Properties and Muxing, for a listing and description of the pin functions and properties.

4 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC5676R.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

4.1 Maximum Ratings

Table 2. Absolute Maximum Ratings[1]

Spec	Characteristic	Symbol	Min	Max[2]	Unit
1	1.2 V Core Supply Voltage[3]	V_{DD}	–0.3	1.65 [4]	V
2	SRAM Standby Voltage	V_{STBY}	–0.3	5.5 [5,6]	V
3	Clock Synthesizer Voltage	V_{DDSYN}	–0.3	4.5 [6,7]	V
4	I/O Supply Voltage (I/O buffers and predrivers)	V_{DD33}	–0.3	4.5 [6,7]	V
5	Analog Supply Voltage (reference to V_{SSA}[8])	V_{DDA}[9]	–0.3	5.5 [5,6]	V
6	I/O Supply Voltage (fast I/O pads)	V_{DDE}	–0.3	4.5 [6]	V
7	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	–0.3	5.5 [5,6]	V
8	Voltage Regulator Input Supply Voltage	V_{DDREG}	–0.3	5.5[5,6]	V
9	Analog Reference High Voltage (reference to V_{RL}[10])	V_{RH}[11]	–0.3	5.5 [5,6]	V
10	V_{SS} to V_{SSA}[8] Differential Voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
11	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	–0.3	5.5 [5,6]	V
12	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
13	V_{DD33} to V_{DDSYN} Differential Voltage	$V_{DD33} – V_{DDSYN}$	–0.1	0.1	V
14	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
15	Maximum Digital Input Current [12] (per pin, applies to all digital pins)	I_{MAXD}	–3 [13]	3 [13]	mA
16	Maximum Analog Input Current [14] (per pin, applies to all analog pins)	I_{MAXA}	–3 [9,13]	3 [9,13]	mA

Table 2. Absolute Maximum Ratings[1] (continued)

Spec	Characteristic	Symbol	Min	Max[2]	Unit
17	Maximum Operating Temperature Range [15] – Die Junction Temperature	T_J	–40.0	150.0	°C
18	Storage Temperature Range	T_{stg}	–55.0	150.0	°C
19	Maximum Solder Temperature [16] Pb-free package SnPb package	T_{sdr}	 — —	 260.0 245.0	°C
20	Moisture Sensitivity Level [17]	MSL	—	3	—

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 1.2 V ±10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

4 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

7 4.5 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

8 MPC5676R has two analog power supply pins on the pinout: VDDA_A and VDDA_B.

9 MPC5676R has two analog ground supply pins on the pinout: VSSA_A and VSSA_B.

10 MPC5676R has two analog low reference voltage pins on the pinout: VRL_A and VRL_B.

11 MPC5676R has two analog high reference voltage pins on the pinout: VRH_A and VRH_B.

12 Total injection current for all pins must not exceed 25 mA at maximum operating voltage.

13 Injection current of ±5 mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25 V maximum analog or V_{DDEH} supply when under this stress condition.

14 Total injection current for all analog input pins must not exceed 15 mA.

15 Lifetime operation at these specification limits is not guaranteed.

16 Solder profile per CDF-AEC-Q100.

17 Moisture sensitivity per JEDEC test method A112.

4.2 Thermal Characteristics

Table 3. Thermal Characteristics, 416-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	24	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	16	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	18	°C/W

Table 3. Thermal Characteristics, 416-pin TEPBGA Package[1] (continued)

Characteristic	Symbol	Value	Unit
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	13	°C/W
Junction to Board [5]	$R_{\theta JB}$	8	°C/W
Junction to Case [6]	$R_{\theta JC}$	4	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	3	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 4. Thermal Characteristics, 516-pin TEPBGA Package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	24	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	17	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	19	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	14	°C/W
Junction to Board [5]	$R_{\theta JB}$	9	°C/W
Junction to Case [6]	$R_{\theta JC}$	5	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

4.3 EMI (Electromagnetic Interference) Characteristics

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to www.nxp.com and perform a keyword search for “radiated emissions.” The following tables list the values of the device's radiated emissions operating behaviors.

Table 5. EMC Radiated Emissions Operating Behaviors: 416 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK off FM off	40 MHz crystal 180 MHz (f_{EBI_CAL} = 46 MHz)	0.15–50	26	dBμV	1
				50–150	30		
				150–500	34		
				500–1000	30		
				IEC and SAE level	I[2]	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK off FM on[4]	40 MHz crystal 180 MHz (f_{EBI_CAL} = 46 MHz)	0.15–50	24	dBμV	1
				50–150	25		
				150–500	25		
				500–1000	21		
				IEC and SAE level	K[5]	—	1,3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 I = 36 dBμV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4 “FM on” = FM depth of ±2%

5 K = 30 dBμV

4.4 ESD Characteristics

Table 6. ESD Ratings[1,2]

Spec	Characteristic	Symbol	Value	Unit
1	ESD for Human Body Model (HBM)	V_{HBM}	2000	V
2	ESD for Charged Device Model (CDM)	V_{CDM}	750 (corners) 500 (other)	V

[1] All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.5 PMC/POR/LVI Electrical Specifications

Table 7. PMC Operating conditions

Spec	Name	Parameter	Condition	Min	Typ	Max	Unit
1	V_{DDREG}	Supply voltage VDDREG 5 V nominal[1]	LDO5V / SMPS5V mode	4.5	5	5.5	V
2	V_{DDREG}	Supply voltage VDDREG 3 V nominal[1]	LDO3V mode	3.0	3.3	3.6	V
3	V_{DD33}	Supply voltage VDDSYN / V_{DD33} 3.3 V nominal[2]	LDO3V mode	3.0	3.3	3.6	V
4	V_{DD}	Supply voltage VDD 1.2 V nominal[3]	—	1.14	1.2	1.32	V

[1] Voltage should be higher than maximum V_{LVDREG} to avoid LVD event

[2] Applies to both V_{DD33} (flash supply) and VDDSYN (PLL supply) pads. Voltage should be higher than maximum V_{LVD33} to avoid LVD event

[3] Voltage should be higher than maximum V_{LVD12} to avoid LVD event

NOTE

In the following table, “untrimmed” means “at reset” and “trimmed” means “after reset”.

Table 8. PMC Electrical Specifications

Spec	Name	Symbol	Condition	Min	Typ	Max	Unit
1	Nominal bandgap reference voltage	V_{BG}	—	0.59	0.620	0.65	V
1a	Bandgap reference voltage during power on reset	—	—	V_{BG} – 5%	V_{BG}	V_{BG} + 5%	V
1b	Bandgap reference voltage at nominal voltage / nominal temperature after power on reset	—	—	V_{BG} – 2%	V_{BG}	V_{BG} + 2%	V

Table 8. PMC Electrical Specifications

Spec	Name	Symbol	Condition	Min	Typ	Max	Unit
1c	Bandgap reference voltage / temperature dependence after power on reset	—	—	—	300	—	ppm/C
1d	Bandgap reference voltage / voltage dependence (V_{DDREG}) after power on reset	—	—	—	1500	—	
2	Nominal VRC regulated 1.2V output VDD[1]	$V_{DD12OUT}$	—	—	1.2	—	V
2a	VRC 1.2V output variation at reset (unloaded)[2]	—	At POR	$V_{DD12OUT}$ – 8%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 10%	
2b	VRC 1.2V output variation after reset(REGCTL load max. 20mA, VDD load max. 1A)	—	After POR	$V_{DD12OUT}$ – 5%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 10%	
2c	Trimming step Vdd1p2	$V_{STEPV12}$	—	—	10	—	mV
3	POR rising VDD 1.2V	V_{PORC}	—	-	0.7	—	V
3a	POR VDD 1.2V variation	—	—	V_{PORC} – 30%	V_{PORC}	V_{PORC} + 30%	
3b	POR 1.2V hysteresis	—	—	—	75	—	mV
4	Nominal rising LVD 1.2V[3]	V_{LVD12}	—	—	1.100	—	V
4a	LVD 1.2V variation before band gap trim[4]	—	At POR	V_{LVD12} – 6%	V_{LVD12}	V_{LVD12} + 6%	
4b	LVD 1.2V variation after band gap trim[4]	—	After POR	V_{LVD12} – 3%	V_{LVD12}	V_{LVD12} + 3%	
4c	LVD 1.2V Hysteresis	—	—	15	20	25	mV
4d	Trimming step LVD 1.2V	$V_{LVDSTEP12}$	—	—	10	—	mV
5	VRC 1.2V max DC output current	I_{REGCTL}	—	—	—	20	mA
6	Voltage regulator 1.2V current consumption VDDREG	—	—	—	3	—	mA
7	Nominal Vreg 3.3V output[5]	$V_{DD33OUT}$	—	—	3.3	—	V
7a	Vreg 3.3V output variation at reset (unloaded)[6]	—	At POR	$V_{DD33OUT}$ – 6%	$V_{DD33OUT}$	$V_{DD33OUT}$ + 10%	
7b	Vreg 3.3V output variation after reset (max. load 60mA)	—	After POR	$V_{DD33OUT}$ – 5%	$V_{DD33OUT}$	$V_{DD33OUT}$ + 10%	
7c	Trimming step VDDSYN	$V_{STEPV33}$	—	—	30	—	mV
8	Nominal rising LVD 3.3V[7]	V_{LVD33}	—	—	2.950	—	V
8a	LVD 3.3V variation before band gap trim[6]	—	At POR	V_{LVD33} – 5%	V_{LVD33}	V_{LVD33} + 5%	
8b	LVD 3.3V variation after bad gap trim[6]	—	After POR	V_{LVD33} – 3%	V_{LVD33}	V_{LVD33} + 3%	

Table 8. PMC Electrical Specifications

Spec	Name	Symbol	Condition	Min	Typ	Max	Unit
8c	LVD 3.3V Hysteresis	—	—	—	30	—	mV
8d	Trimming step LVD 3.3V	$V_{LVDSTEP33}$	—	—	30	—	mV
9	Vreg 3.3V minimum peak DC output current supplied by regulator without causing V_{LVD33}[8]	I_{DD33}	—	60	—	—	mA
10	Voltage regulator 3.3V current consumption VDDREG[9]	—	—	—	2	—	mA
11	POR rising on VDDREG	V_{PORREG}	—	—	2.00	—	V
11a	POR VDDREG variation	—	—	V_{PORREG} – 30%	V_{PORREG}	V_{PORREG} + 30%	
11b	POR VDDREG hysteresis	—	—	—	250	—	mV
12	Nominal rising LVD VDDREG	V_{LVDREG}	LDO3V / LDO5V mode	—	2.950	—	V
12a	LVD VDDREG variation at reset[10]	—	At POR	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	
12b	LVD VDDREG variation after reset[10]	—	After POR	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	
12c	LVD VDDREG Hysteresis	—	LDO3V / LDO5V mode	—	30	—	mV
12d	Trimming step LVD VDDREG	$V_{LVDSTEPREG}$	LDO3V / LDO5V mode	—	30	—	mV
13	Nominal rising LVD VDDREG	V_{LVDREG}	SMPS5V mode	—	4.360	—	V
13a	LVD VDDREG variation at reset[10]	—	At POR	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	
13b	LVD VDDREG variation after reset[10]	—	After POR	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	
14	SMPS regulator output resistance[11]	—	—	—	15	25	Ohm
15	SMPS regulator clock frequency	—	After POR	1.0	1.5	—	MHz
16	SMPS regulator overshoot at start-up[12]	—	GBD/GBC[13]	—	1.32	1.4	V
17	SMPS maximum output current, as required by SoC[14]	—	—	—	1.0	—	A
18	Voltage variation on current step (20% to 80% of maximum current with 4 usec constant time)[14]	—	GBD/GBC[13]	—	—	0.1	V

[1] Nominal internal regulator output voltage is 1.27V
[2] Voltage should be higher than maximum VLVD12 to avoid LVD event
[3] ~VDD12OUT *0.87
[4] Rising VDD
[5] Nominal internal regulator output voltage is 3.4V
[6] Rising VDDSYN
[7] ~VDD33OUT *0.872
[8] VDDSYN
[9] Except IDD33
[10] Rising VDDREG
[11] Pull up to VDDREG when high, pull down to VSSREG when low.
[12] Depends on external device, can be as high as 1.6V for short time (<100 usec each start-up)
[13] GBD — Guaranteed By Design; GBC — Guaranteed by Characterization
[14] Proper external devices required

4.5.1 Regulator Example

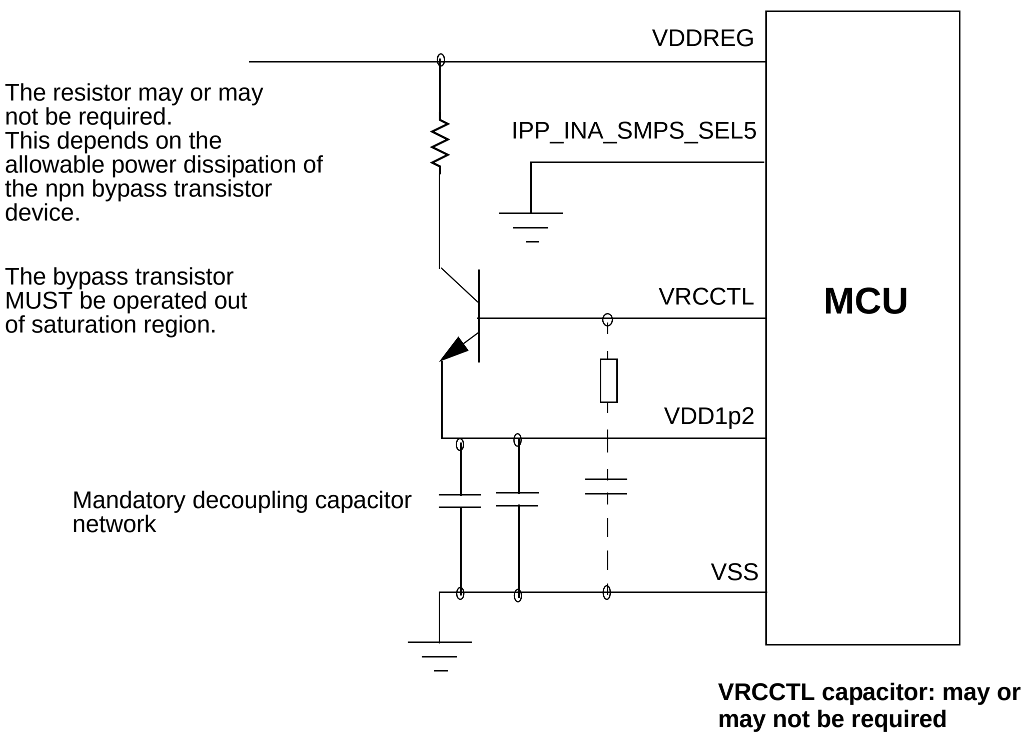


Figure 5. VRC 1.2 V LDO configuration with external bipolar

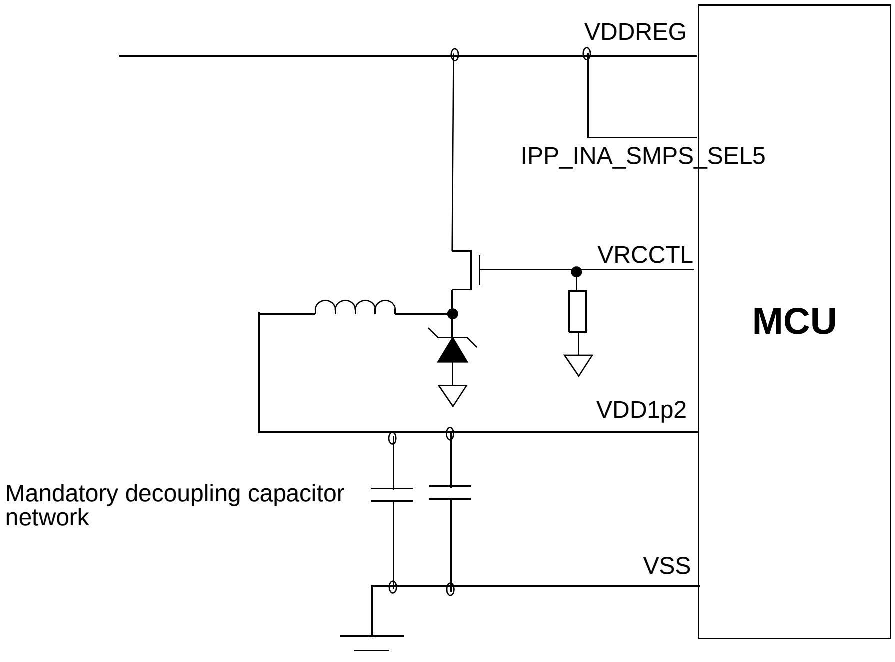


Figure 6. VRC 1.2V buck SMPS LDO configuration with external MOS - Schottky diode

Table 9. VRC LDO recommended external devices

Part Name	Part Type	Nominal	Description
NJD2873 Beta (Bf) Vbe Vce	NPN Capacitor	 6 x 4.7 uF - 20 V	ON Semiconductor TM From 60 to 550 From 0.4 V to 1.0 V From 0.2 V to 0.6 V depends on package / power Ceramic low ESR—One for each VDD pin
	Capacitor	6 x 0.1 uF - 20 V	Ceramic —One capacitor for each VDD pin
	Capacitor	20 uF	Supply decoupling cap (close to bipolar collector)
	Capacitor	2.2 uF	Snubber cap, required with NJD2873 (on bipolar base)
	Resistor	12 Ω	Optional ESR for snubber cap

Table 10. VRC SMPS recommended external devices

Part Name	Part Type	Nominal	Description
IR7353	HS nMOS + Schottky		Low threshold n-MOS/Low Vf Schottky diode
SS8P3L	Schottky		Low Vf Schottky diode
Vf			From 0.4V to 0.6 V
SI3460 or equivalent	nMOS		Low threshold n-MOS
Vth			Less than 2 V
Ids			More than 1.5 A
Vds			More than 12 V
Rdson			Less than 100 Ohms
Cg			Less than 5 nF
Turn on / off delay			Less than 50 ns
Rise time			Less than 90 ns
LQH66SN2R2M03	inductor	2.2 uH—3.2 A	muRata TM shielded coil, preferred f_{max} > 40 MHz
C3225X7R1E106M	capacitor	22 uF — 25 V	TDK high capacitance ceramic SMD (on VDD close to coil)
C3225X7R1E225K	capacitor	2 to 6 x 2.2 uF — 25 V	TDK ceramic SMD (on VDD close to MCU)
	capacitor	6 x 0.1 uF — 20 V	Ceramic -One capacitor for each VDD pin
C3225X7R1E106M	capacitor	22 uF — 25 V	Supply decoupling cap—close to n-MOS drain
	resistor	20 K	Pull down for power n—MOS gate

4.6 Power Up/Down Sequencing

There is no power sequencing required among power sources during power up and power down in order to operate within specification as long as the following two rules are met:

- When VDDREG is tied to a nominal 3.3V supply, VDD33 and VDDSYN must be both shorted to VDDREG.
- When VDDREG is tied to a 5V supply, VDD33 and VDDSYN must be tied together and shall be powered by the internal 3.3V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each V_{DDE}/V_{DDEH} first and then power up V_{DD}. For power down, drop V_{DD} to 0 V first, and then drop all V_{DDE}/V_{DDEH} supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to Table 11 and Table 12.

Table 11. Power Sequence Pin States for MH and AE pads

VDD	VDD33	VDDE	MH Pad	MH+LVDS Pads[1]	AE/up-down Pads
High	High	High	Normal operation	Normal operation	Normal operation
—	Low	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs driven high	Pull-ups enabled, pull-downs disabled
Low	High	Low	Output low, pin unpowered	Outputs disabled	Output low, pin unpowered
Low	High	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled

1 MH+LVDS pads are output-only.

Table 12. Power Sequence Pin States for F and FS pads

VDD	VDD33	VDDE	F and FS pads
low	low	high	Outputs drive high
low	high	—	Outputs Disabled
high	low	low	Outputs Disabled
high	low	high	Outputs drive high
high	high	low	Normal operation - except no drive current and input buffer output is unknown.[1]
high	high	high	Normal Operation

1 The pad pre-drive circuitry will function normally but since VDDE is unpowered the outputs will not drive high even though the output pmos can be enabled.

4.6.1 Power-Up

If V_{DDE}/V_{DDEH} is powered up first, then a threshold detector tristates all drivers connected to V_{DDE}/V_{DDEH}. There is no limit to how long after V_{DDE}/V_{DDEH} powers up before V_{DD} must power up. If there are multiple V_{DDE}/V_{DDEH} supplies, they can be powered up in any order. For each V_{DDE}/V_{DDEH} supply not powered up, the drivers in that V_{DDE}/V_{DDEH} segment exhibit the characteristics described in the next paragraph.

If V_{DD} is powered up first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DD} powers up before V_{DDE}/V_{DDEH} must power up.

The rise times on the power supplies are to be no faster than 25 V/millisecond.

4.6.2 Power-Down

If V_{DD} is powered down first, then all drivers are tristated. There is no limit to how long after V_{DD} powers down before V_{DDE}/V_{DDEH} must power down.

If V_{DDE}/V_{DDEH} is powered down first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DDE}/V_{DDEH} powers down before V_{DD} must power down.

There are no limits on the fall times for the power supplies.

4.6.3 Power Sequencing and POR Dependent on V_{DDA}

During power up or down, V_{DDA} can lag other supplies (of magnitude greater than $V_{DDEH}/2$) within 1 V to prevent any forward-biasing of device diodes that causes leakage current and/or POR. If the voltage difference between V_{DDA} and V_{DDEH} is more than 1 V, the following will result:

- Triggers POR (ADC monitors on V_{DDEH1} segment which powers the RESET pin) if the leakage current path created, when V_{DDA} is sufficiently low, causes sufficient voltage drop on V_{DDEH1} node monitored crosses low-voltage detect level.
- If V_{DDA} is between 0–2 V, powering all the other segments (especially V_{DDEH1}) will not be sufficient to get the part out of reset.
- Each V_{DDEH} will have a leakage current to V_{DDA} of a magnitude of (($V_{DDEH} - V_{DDA}$ – 1 V(diode drop)/200 KOhms) up to ($V_{DDEH}/2 = V_{DDA} + 1$ V). .
- Each V_{DD} has the same behavior; however, the leakage will be small even though there is no current limiting resistor since V_{DD} = 1.32 V max.

4.7 DC Electrical Specifications

Table 13. DC Electrical Specifications[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	Core Supply Voltage (External Regulation)	V_{DD}	1.14	1.32[2, 3]	V
1a	Core Supply Voltage (Internal Regulation)[4]	V_{DD}	1.08	1.32	V
2	I/O Supply Voltage (fast I/O pads)	V_{DDE}	3.0	3.6[2]	V
3	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	3.0	5.25[2]	V
4	3.3 V I/O Buffer Voltage	V_{DD33}	3.0	3.6[2]	V
5	Analog Supply Voltage	V_{DDA}	4.75	5.25[2]	V
6a	SRAM Standby Voltage low range	V_{STBY_LOW}	0.95[5]	1.2	V
6b	SRAM Standby Voltage high range	V_{STBY_HIGH}	2	6	V
7	Voltage Regulator Control Input Voltage[6]	V_{DDREG}	2.7[7]	5.5[2]	V
8	Clock Synthesizer Operating Voltage[8]	V_{DDSYN}	3.0	3.6[2]	V
9	Fast I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_F}	 $0.65 \times V_{DDE}$ $0.55 \times V_{DDE}$	$V_{DDE} + 0.3$	V
10	Fast I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_F}	$V_{SS} - 0.3$	 $0.35 \times V_{DDE}$ $0.40 \times V_{DDE}$	V
11	Medium I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_S}	 $0.65 \times V_{DDEH}$ $0.55 \times V_{DDEH}$	$V_{DDEH} + 0.3$	V

Table 13. DC Electrical Specifications[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
12	Medium I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_S}	$V_{SS} - 0.3$	 $0.35 \times V_{DDEH}$ $0.40 \times V_{DDEH}$	V
13	Fast I/O Input Hysteresis	V_{HYS_F}	$0.1 \times V_{DDE}$	—	V
14	Medium I/O Input Hysteresis	V_{HYS_S}	$0.1 \times V_{DDEH}$	—	V
15	Analog Input Voltage	V_{INDC}	$V_{SSA} - 0.1$	$V_{DDA} + 0.1$	V
16	Fast I/O Output High Voltage[9]	V_{OH_F}	$0.8 \times V_{DDE}$	—	V
17	Medium I/O Output High Voltage[10]	V_{OH_S}	$0.8 \times V_{DDEH}$	—	V
18	Fast I/O Output Low Voltage[9]	V_{OL_F}	—	$0.2 \times V_{DDE}$	V
19	Medium I/O Output Low Voltage	V_{OL_S}	—	$0.2 \times V_{DDEH}$[10] $0.15 \times V_{DDEH}$[11]	V
20	Load Capacitance (Fast I/O)[12] DSC(PCR[8:9]) = 0b00 DSC(PCR[8:9]) = 0b01 DSC(PCR[8:9]) = 0b10 DSC(PCR[8:9]) = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF
21	Input Capacitance (Digital Pins)	C_{IN}	—	7	pF
22	Input Capacitance (Analog Pins)	C_{IN_A}	—	10	pF
23	Input Capacitance (Digital and Analog Pins[13])	C_{IN_M}	—	12	pF
24	Operating Current 1.2 V Supplies @ f_{sys} = 180 MHz V_{DD} (including V_{DDF} current)@1.32 V V_{STBY}[14] @1.2 V and 85°C V_{STBY} @6.0 V and 85°C V_{DDF}[15] (P/E) V_{DDF}[15] (Read) V_{DDF}[15] (RWW) V_{DDF}[15] (Standby) V_{DDF}[15] (Disabled)	 I_{DD} I_{DDSTBY} $I_{DDSTBY6}$ I_{DDFPE} $I_{DDFREAD}$ I_{DDFRWW} $I_{DDplTANDBY}$ $I_{DDFDISABLED}$	 — — — — — — — —	 1.0[16] 0.10 0.15 36[17] 50[17] 90[17] 0.20[17] 0.10[17]	 A mA mA mA mA mA mA mA
25	Operating Current 3.3 V Supplies @ f_{sys} = 180 MHz V_{DD33}[18] V_{DDSYN} V_{FLASH}[19] (P/E) V_{FLASH}[19] (Read) V_{FLASH}[19] (RWW) V_{FLASH}[19] (Standby) V_{FLASH}[19] (Disabled)	 I_{DD33} I_{DDSYN} $I_{DDFLASHPE}$ $I_{DDFLASHREADS}$ $I_{DDFLASHRWW}$ $I_{DDFLASHSTANDBY}$ $I_{DDFLASHDISABLED}$	 — — — — — — —	 note[18] 7[20] 32[21] 6.4[21] 40[21] 3.4[21] 0.10[21]	 mA mA mA mA mA mA mA
26	Operating Current 5.0 V Supplies @ f_{sys} = 180 MHz V_{DDA} Analog Reference Supply Current (Transient) V_{DDREG}	 I_{DDA} I_{REF} I_{REG}	 — — —	 50[22] 1.0 22	 mA mA mA

Table 13. DC Electrical Specifications[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
27	Operating Current V_{DDE}/V_{DDEH}[23] Supplies V_{DDE2} V_{DDEH1} V_{DDEH3} V_{DDEH4} V_{DDEH5} V_{DDEH6} V_{DDEH7}	 I_{DD2} I_{DD1} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7}	 — — — — — — —	note[23]	 mA mA mA mA mA mA mA
28	Fast I/O Weak Pull Up/Down Current[24] 3.0 V–3.6 V	I_{ACT_F}	42	158	µA
29	Medium I/O Weak Pull Up/Down Current[25] 3.0 V–3.6 V 4.5 V–5.5 V	I_{ACT_S}	 15 35	 95 200	 µA µA
30	I/O Input Leakage Current[26]	I_{INACT_D}	–2.5	2.5	µA
31	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
32	Analog Input Current, Channel Off[27], AN[0:7], AN38, AN39 Analog Input Current, Channel Off, all other analog inputs AN[x] = -/+ 150nA	I_{INACT_A}	–250 –150	250 150	nA nA
33	V_{SS} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
34	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 100	mV
35	V_{RL} Differential Voltage	$V_{RL} – V_{SSA}$	–100	100	mV
36	Analog Reference High Voltage	V_{RH}	V_{DDA} – 100	V_{DDA}	mV
37	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	4.75	5.25	V
38	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–100	100	mV
39	Operating Temperature Range—Ambient (Packaged)	T_A (T_L to T_H)	–40.0	125.0	°C
40	Slew rate on power supply pins	—	—	25	V/ms
41	Weak Pull-Up/Down Resistance[28,29] 200 kΩ Option	$R_{PUPD200K}$	130	280	kΩ
42	Weak Pull-Up/Down Resistance[28,29] 100 kΩ Option	$R_{PUPD100K}$	65	140	kΩ
43	Weak Pull-Up/Down Resistance[28] (5 kΩ Option) 5 V ± 10% supply 3.3 V ± 10% supply	R_{PUPD5K}	 1.4 1.7	 5.2 7.7	kΩ
44	Pull-Up/Down Resistance Matching Ratios (100K/200K) (Pull-up and pull-down resistances both enabled and settings are equal)	$R_{PUPDMATCH}$	–2.5	2.5	%

1 These specifications are design targets and subject to change per device characterization.

2 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

3 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

4 Assumed with DC load.

5 V_{STBY} below 0.95 V the RAM will not retain states, but will be operational. V_{STBY} can be 0 V when bypass standby mode.

6 Regulator is functional with derated performance, with supply voltage down to 4.0 V for system with V_{DDREG} = 4.5 V (min).

7 2.7 V minimum operating voltage allowed during vehicle crank for system with V_{DDREG} = 3.0 V (min). Normal operating voltage should be either V_{DDREG} = 3.0 V (min) or 4.5 V (min) depending on the user regulation voltage system selected.

8 Required to be supplied when 3.3 V regulator is disabled. See Section 4.5, "PMC/POR/LVI Electrical Specifications."

9 I_{OH_F} = {12,20,30,40} mA and I_{OL_F} = {24,40,50,65} mA for {00,01,10,11} drive mode with V_{DDE}= 3.0 V.

10 I_{OH_S} = {11.6} mA and IOL_S = {17.7} mA for {medium} I/O with V_{DDEH} = 4.5 V;
I_{OH_S} = {5.4} mA and IOL_S = {8.1} mA for {medium} I/O with V_{DDEH} = 3.0 V

11 I_{OL_S}= 2 mA

12 Applies to D_CLKOUT, external bus pins, and Nexus pins.

13 Applies to the FCK, SDI, SDO, and SDS_B pins.

14 V_{STBY} current specified at 1.0 V at a junction temperature of 85 ^{o}C. V_{STBY} current is 700 µA maximum at a junction temperature of 150 ^{o}C.

15 VDDF pin is shorted to V_{DD} on the package substrate.

16 Preliminary. Specification pending typical and/or high-use Runidd pattern simulation as well as final silicon characterization. 1.0 A based on transistor count estimate at Worst Case (wcs) process and temperature condition.

17 Typical values from the simulation.

18 Power requirements for the V_{DD33} supply depend on the frequency of operation and load of all I/O pins, and the voltages on the I/O segments. See Section 4.7.2, "I/O Pad V_{DD33} Current Specifications," for information on both fast (F, FS) and medium (MH) pads. Also refer to Table 15 for values to calculate power dissipation for specific operation.

19 VFLSH pin is shorted to V_{DD33} on the package substrate.

20 This value is a target that is subject to change.

21 Typical values from the simulation.

22 These value allows a 5 V 20 mA reference to supply ADC + REF.

23 Power requirements for each I/O segment depend on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Section 4.7.1, "I/O Pad Current Specifications," for information on I/O pad power. Also refer to Table 14 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

24 Absolute value of current, measured at V_{IL} and V_{IH}.

25 Absolute value of current, measured at V_{IL} and V_{IH}.

26 Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types F and MH.

27 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types AE and AE/up-down.

28 This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

29 When the pull-up and pull-down of the same nominal 200 kΩ or 100 kΩ value are both enabled, assuming no interference from external devices, the resulting pad voltage will be 0.5*V_{DDEH} ± 2.5%.

4.7.1 I/O Pad Current Specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 14 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 14.

The AC timing of these pads are described in the Section 4.11.2, "Pad AC Specifications."

Table 14. V_{DDE}/V_{DDEH} I/O Pad Average DC Current[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{DRV_MH}	50	50	5.25	11	16.0
2			20	50	5.25	01	6.3
3			3.0	50	5.25	00	1.1
4			2.0	200	5.25	00	2.4
5	Fast	I_{DRV_FC}	66	10	3.6	00	6.5
6			66	20	3.6	01	9.4
7			66	30	3.6	10	10.8
8			66	50	3.6	11	33.3
9			66	10	1.98	00	2.0
10			66	20	1.98	01	3.0
11			66	30	1.98	10	4.4
12			66	50	1.98	11	15.1
13	Fast w/ Slew Control	I_{DRV_FSR}	66	50	3.6	11	12.0
14			50	50	3.6	10	6.2
15			33.33	50	3.6	01	4.0
16			20	50	3.6	00	2.4
17			20	200	3.6	00	8.9

1 These are average IDDE numbers for worst case PVT from simulation. Currents apply to output pins only.

2 All loads are lumped.

4.7.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The V_{DD33} current draw on fast speed pads can be calculated from Table 15 dependent on the voltage, frequency, and load on all F type pins. The V_{DD33} current draw on medium pads can be calculated from Table 15 dependent on voltage and independent on the frequency and load on all MH type pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 15.

The AC timing of these pads are described in the Section 4.11.2, "Pad AC Specifications."

Table 15. V_{DD33} Pad Average DC Current[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{33_MH}	—	—	3.6	5.5	—	0.0007
2	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.92
3			66	20	3.6	3.6	01	1.14
4			66	30	3.6	3.6	10	1.50
5			66	50	3.6	3.6	11	2.19
6			66	10	3.6	1.98	00	0.70
7			66	20	3.6	1.98	01	0.90
8			66	30	3.6	1.98	10	1.08
9			66	50	3.6	1.98	11	1.52
10	Fast w/ Slew Control	I_{33_FSR}	66	50	3.6	3.6	11	0.74
11			50	50	3.6	3.6	10	0.52
12			33.33	50	3.6	3.6	01	0.36
13			20	50	3.6	3.6	00	0.19
14			20	200	3.6	3.6	00	0.19

1 These are average IDD33 for worst case PVT from simulation. Currents apply to output pins only for the fast pads and to input pins only for the medium pads.

2 All loads are lumped.

4.7.3 LVDS Pad Specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol, which is an enhanced feature of the DSPI module.

Table 16. DSPI LVDS Pad Specification [1, 2]
(V_{DD33} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, $T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
Data Rate						
1	Data Frequency	$f_{LVDSCLK}$	—	—	40	MHz
Driver Specs						
2	Differential Output Voltage SRC=0b00 or 0b11 SRC=0b01 SRC=0b10	V_{OD}	 215 170 260	—	 400 320 480	mV
3	Common Mode Voltage (LVDS), VOS	V_{OS}	1.075	1.2	1.325	V
4	Rise/Fall Time	t_R or t_F	—	—	2.5	ns
5	Delay, Z to Normal (High/Low)	t_{DZ}	—	—	100	ns

Table 16. DSPI LVDS Pad Specification [1, 2] (continued)
(V_{DD33} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, T_A = T_L to T_H)

6	Differential Skew between Positive and Negative LVDS Pair $\lvert t_{phla} - t_{plhb} \rvert$ or $\lvert t_{plhb} - t_{phla} \rvert$	t_{Skew}	—	—	0.5	ns
Termination						
7	Termination Resistance[3]	R_{Load}	95	100	105	ohm
8	Load	—	—	—	32	pF

[1] These are typical values that are estimated from simulation.
[2] These specifications are subject to change per device characterization.
[3] The termination resistance spec is not meant to specify the receiver termination requirements. They are there to establish the measurement criteria for the specs in this table. As per the TIA/EIA-644A standard, the LVDS receiver termination resistance can vary from 90 to 132 Ω .

4.8 Oscillator and FMPLL Electrical Characteristics

Table 17. FMPLL Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[2] (Normal Mode) Crystal Reference (PLLCFG2 = 0b0) Crystal Reference (PLLCFG2 = 0b1) External Reference (PLLCFG2 = 0b0) External Reference(PLLCFG2 = 0b1)	 $f_{ref\_crystal}$ $f_{ref\_crystal}$ f_{ref_ext} f_{ref_ext}	 8 40 8 40	 20 40[3] 20 40	MHz
2	PLL Frequency [4] Enhanced Mode	f_{PLL}	$f_{vco(min)} \div 64$	f_{max}	MHz
3	Loss of Reference Frequency[5]	f_{LOR}	100	1000	kHz
4	Self Clocked Mode Frequency[6]	f_{SCM}	4	16	MHz
5	PLL Lock Time[7]	t_{LPLL}	—	<750	µs
6	Duty Cycle of Reference [8, 9]	t_{DC}	40	60	%
7	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{sys}
8	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{sys}
9	D_CLKOUT Period Jitter[10, 11] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{clkout}
10	Peak-to-Peak Frequency Modulation Range Limit [12,13] (f_{sys} Max must not be exceeded)	C_{mod}	0	4	%f_{sys}
11	FM Depth Tolerance[14]	C_{mod_err}	–0.25	0.25	%f_{sys}
12	VCO Frequency	f_{VCO}	192	600	MHz
13	Modulation Rate Limits[15]	f_{mod}	0.400	1	MHz
14	Predivider Operating Frequency	f_{prediv}	4	10	MHz

1 All values given are initial design targets and subject to change.

2 Crystal and External reference frequency limits depend on device relying on PLL to lock prior to release of reset, default PREDIV/EPREDIV, MFD/EMFD default settings, and VCO frequency range. Absolute minimum loop frequency is 4 MHz.

3 Upper tolerance of less than 1% is allowed on 40MHz crystal.

4 All internal registers retain data at 0 Hz.

5 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

6 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}. This frequency is measured at D_CLKOUT with the divider set to divide-by-2 of the system clock. NOTE: in SCM, the PLL is running open loop at a centercode 0x4. The MFD has no effect and the RFD is bypassed.

7 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

8 For FlexRay operation, duty cycle requirements are higher.

9 Duty cycle can be 20–80% when PLL is used with a pre-divider greater than 1.

10 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval. D_CLKOUT divider set to divide-by-2.

11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of $C_{jitter} + C_{mod}$.

12 Modulation depth selected must not result in f_{pll} value greater than the f_{pll} maximum specified value.

13 Maximum and minimum variation from programmed modulation depth is pending characterization. Depth settings available in control register are: 1%, 2%, 3%, and 4% peak-to-peak.

14 Depth tolerance is the programmed modulation depth ±0.25% of F_{sys}. Initial design target pending silicon evaluation.

15 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

Table 18. Oscillator Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, $V_{SS} = V_{SSSYN}$ = 0 V, $T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Crystal Mode Differential Amplitude[2] (Min differential voltage between EXTAL and XTAL)	$V_{crystal\_diff\_amp}$	$\lvert V_{extal} - V_{xtal} \rvert > 0.4$ V	—	V
2	Crystal Mode: Internal Differential Amplifier Noise Rejection	$V_{crystal\_diff\_amp\_nr}$	—	$\lvert V_{extal} - V_{xtal} \rvert < 0.2$ V	V
3	EXTAL Input High Voltage Bypass mode, External Reference	V_{IHEXT}	$((V_{DD33}/2) + 0.4$ V)	—	V
4	EXTAL Input Low Voltage Bypass mode, External Reference	V_{ILEXT}	—	$(V_{DD33}/2) - 0.4$ V	V
5	XTAL Current[3]	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF

Table 18. Oscillator Electrical Specifications[1] (continued)
(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal spec	See crystal spec	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[4]$)$	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$(2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[4]$)$	pF

1 All values given are initial design targets and subject to change.
2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criterion has to be met for oscillator's comparator to produce output clock.
3 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.
4 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

4.9 eQADC Electrical Characteristics

Table 19. eQADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency	f_{ADCLK}	2	16	MHz
2	Conversion Cycles	CC	2 + 13	128 + 14	ADCLK cycles
3	Stop Mode Recovery Time[1]	T_{SR}	10	—	µs
4	Resolution[2]	—	1.25	—	mV
5	INL: 8 MHz ADC Clock[3]	INL8	–4[4]	4[4]	LSB[5]
6	INL: 16 MHz ADC Clock[3]	INL16	–8[4]	8[4]	LSB
7	DNL: 8 MHz ADC Clock[3]	DNL8	–3[4]	3[4]	LSB
8	DNL: 16 MHz ADC Clock[3]	DNL16	–3[4]	3[4]	LSB
9	Offset Error without Calibration	OFFNC	0[4]	100[4]	LSB
10	Offset Error with Calibration	OFFWC	–4[4]	4[4]	LSB
11	Full Scale Gain Error without Calibration	GAINNC	–120[4]	0[4]	LSB
12	Full Scale Gain Error with Calibration	GAINWC	–4[4,6]	4[4,6]	LSB
13	Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–1	1	mA
14	Incremental Error due to injection current[11, 12]	E_{INJ}	—	±4[4]	Counts
15	TUE value at 8 MHz [13, 14] (with calibration)	TUE8	—	±4[4,6]	Counts

Table 19. eQADC Conversion Specifications (Operating) (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
16	TUE value at 16 MHz [13, 14] (with calibration)	TUE16	—	±8	Counts
17	Variable gain amplifier accuracy (gain=1)[15] INL, 8 MHz ADC INL, 16 MHz ADC DNL, 8 MHz ADC DNL, 16 MHz ADC	GAINVGA1	 –4 –8 –3[16] –3[16]	 4 8 3[16] 3[16]	Counts[17]
18	Variable gain amplifier accuracy (gain=2)[15] INL, 8 MHz ADC INL, 16 MHz ADC DNL, 8 MHz ADC DNL, 16 MHz ADC	GAINVGA2	 –5 –8 –3 –3	 5 8 3 3	Counts
19	Variable gain amplifier accuracy (gain=4)[15] INL, 8 MHz ADC INL, 16 MHz ADC DNL, 8 MHz ADC DNL, 16 MHz ADC	GAINVGA4	 –7 –8 –4 –4	 7 8 4 4	Counts

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

8 Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.

10 Condition applies to two adjacent pins at injection limits.

11 Performance expected with production silicon.

12 All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ}=I_{INJMAX},I_{INJMIN}$.

13 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

14 TUE does not apply to differential conversions.

15 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

16 Guaranteed 10-bit mono tonicity.

17 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

4.9.1 ADC Internal Resource Measurements

Table 20. Power Management Control (PMC) Specification

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
PMC Normal Mode						
1	Bandgap 0.62 V ADC0 channel 145	V_{ADC145}	0.59	0.62	0.65	V
2	Bandgap 1.2 V ADC0 channel 146	V_{ADC146}	1.10	1.22	1.34	V
3	Vreg1p2 Feedback ADC0 channel 147	V_{ADC147}	V_{DD}/2.147	V_{DD} / 2.045	V_{DD}/1.943	V
4	LVD 1.2 V ADC0 channel 180	V_{ADC180}	V_{DD}/1.863	V_{DD} / 1.774	V_{DD}/1.685	V
5	Vreg3p3 Feedback ADC0 channel 181	V_{ADC181}	Vreg3p3 / 5.733—	Vreg3p3 / 5.460	Vreg3p3 / 5.187	V
6	LVD 3.3 V ADC0 channel 182	V_{ADC182}	Vreg3p3 / 4.996	Vreg3p3 / 4.758	Vreg3p3 / 4.520	V
7	LVD 5.0 V ADC0 channel 183 — LDO mode — SMPS mode	V_{ADC183}	V_{DDREG} / 4.996 V_{DDREG} / 7.384	V_{DDREG} / 4.758 V_{DDREG}/7.032	V_{DDREG} / 4.520 V_{DDREG} / 6.680	V

Table 21. Standby RAM Regulator Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode						
1	Standby Regulator Output ADC1 channel 194	V_{ADC194}	—	1.2	—	V
2	Standby Source Bias ADC1 channel 195	V_{ADC195}	150	—	360	mV

Table 22. ADC Band Gap Reference / LVI Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	—	1.220	—	V

Table 23. Temperature Sensor Electrical Specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$ [1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	-20	—	+20	°C

1 Slope is the measured voltage change per °C.

4.10 C90 Flash Memory Electrical Characteristics

Table 24. Flash Program and Erase Specifications (Pending Si characterization)

Spec	Characteristic	Symbol	Typ[1]	Initial Max[2]	Lifetime Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	38	—	500	µs
2	Page (128 bits) Program Time[4]	$t_{pprogram}$	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	270	1000	5000	ms
4	48 KB Block Pre-program and Erase Time	$t_{48kpperase}$	625	1500	5000	ms
5	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	800	1800	5000	ms
6	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	1500	2600	7500	ms
7	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	3000	5200	15000	ms

1 Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. These values are characterized, but not tested.

2 Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for < 100 program/erase cycles, nominal supply values and operation at 25 °C. These values are verified at production test.

3 Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.

4 Program times are actual hardware programming times and do not include software overhead.

NOTE

The low, mid, and high address blocks of the flash arrays are erased (all bits set to 1) before leaving the factory.

Table 25. Flash Memory AC Timing Specifications[1]

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
T_{RES}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low	—	—	100	ns
T_{DONE}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared	—	—	5	ns
T_{PSRT}	Time between program suspend resume and the next program suspend request.[2]	100	—	—	µs
T_{ESRT}	Time between erase suspend resume and the next erase suspend request.[3]	10	—	—	ms

1 This parameter is guaranteed by characterization before qualification rather than 100% tested.

2 Repeated suspends at a high frequency may result in the operation timing out, and the flash module will respond by completing the operation with a fail code (MCR[PEG] = 0), or the operation not able to finish (MCR[DONE] = 1 during Program operation). The minimum time between suspends to ensure this does notoccur is T_{PSRT}.

3 If Erase suspend rate is less than T_{ESRT}, an increase of slope voltage ramp occurs during erase pulse. This improves erase time but reduces cycling figure due to overstress.

Table 26. Flash EEPROM Module Life

Spec	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of Program/Erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
2	Number of Program/Erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range (T_J)	P/E	1,000	100,000	cycles
3	Minimum Data Retention at 85 °C ambient temperature[2] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	Retention	 20 10 1 – 5	—	years

1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the NXP definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 27. BIUCR1/BIUCR3 Settings

Spec	Maximum Frequency (MHz)		APC = RWSC	WWSC	DPFEN[1]	IPFEN[1]	PFLIM[2]	BFEN[3]
	Core f_{sys}	Platform f_{platf}						
1	180 MHz	90 MHz	0b010	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
Default setting after reset:			0b111	0b11	0b00	0b00	0b00	0b0

1 For maximum flash performance, set to 0b1.
2 For maximum flash performance, set to 0b10.
3 For maximum flash performance, set to 0b1.

4.11 AC Specifications

4.11.1 Clocking Modes

There are two main modes of operating frequency settings:

- Double 2:1 (Core:Platform) Mode—the core is running at the system frequency setting while the platform and eTPU are running at half the core frequency (system frequency divided by 2).
- eTPU Mode—the core and eTPU are running at the system frequency setting while the platform is running at half the core frequency (system frequency divided by 2).

Table 28 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings.

Table 28. MPC5676R Block Operating Frequency[1, 2]

Spec	Blocks	Symbol	Double Mode Freq (MHz)	eTPU Mode Freq (MHz)
1	Cores	f_{sys} ($t_{cycsys} = 1/f_{sys}$)	$f_{sys} = 180$	$f_{sys} = 180$
2	Platform	f_{platf} ($t_{cyc} = 1/f_{platf}$)	$f_{sys} / 2$	$f_{sys} / 2$
3	eTPU	f_{eTPU}	$f_{sys} / 2$	f_{sys}
4	EBI	f_{ebi}	$f_{sys} / 4$	$f_{sys} / 4$

1 The values in the table are specified at V_{DD} = 1.02 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 4.5 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.
2 Up to the maximum frequency rating of the device (refer to Table 1). The f_{sys} speed is the nominal maximum frequency.

4.11.2 Pad AC Specifications

Table 29. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,4] L → H/H → L (ns)	Rise/Fall[3,4] (ns)	Load Drive (pF)
1	Medium[5]	00	152/165	70/74	50
2			205/220	96/96	200
3		01	28/34	12/15	50
4			52/59	28/31	200
5		11	12/12	5.3/5.9	50
6			32/32	22/22	200
7	Fast[6]	00	2.5	1.2	10
8		01			20
9		10			30
10		11			50
11	Fast with Slew Rate	00	40/40	16/16	50
12			50/50	21/21	200
13		01	13/13	5/5	50
14			19/19	8/8	200
15		10	8/8	2.4/2.4	50
16			12/12	5/5	200
17		11	5/5	1.1/1/1	50
18			8/8	2.6	200
19	Pull Up/Down (3.6 V max)	—	—	7500	50
20	Pull Up/Down (5.25 V max)	—	6000	5000/5000	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.02 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, T_A = T_L to T_H.
2 This parameter is supplied for reference and is not guaranteed by design and not tested.
3 This parameter is guaranteed by characterization before qualification rather than 100% tested.
4 Delay and rise/fall are measured to 20% or 80% of the respective signal.
5 Out delay is shown in Figure 7. Add a maximum of one system clock to the output delay for delay with respect to system clock.
6 Out delay is shown in Figure 7. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 30. Derated Pad AC Specifications (V_{DDEH} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,3] L → H/H → L (ns)	Rise/Fall[4,3] (ns)	Load Drive (pF)
1	Medium[5]	00	200/210	86/86	50
2			270/285	120/120	200
3		01	37/45	15.5/19	50
4			69/82	38/43	200
5		11	18/17	7.6/8.5	50
6			46/49	30/34	200

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, T_A = T_L to T_H.
2 This parameter is supplied for reference and is not guaranteed by design and not tested.
3 Delay and rise/fall are measured to 20% or 80% of the respective signal.
4 This parameter is guaranteed by characterization before qualification rather than 100% tested.
5 Out delay is shown in Figure 7. Add a maximum of one system clock to the output delay for delay with respect to system clock.

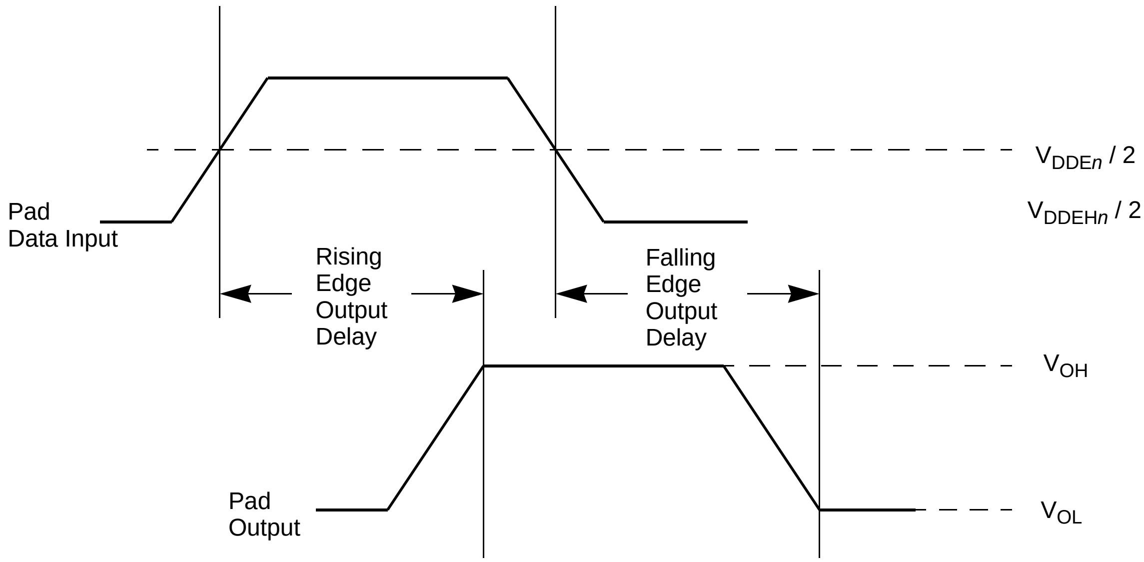


Figure 7. Pad Output Delay

4.12 AC Timing

4.12.1 Generic Timing Diagrams

The generic timing diagrams in Figure 8 and Figure 9 apply to all I/O pins with pad types F and MH. See Table 39 for the pad type for each pin.

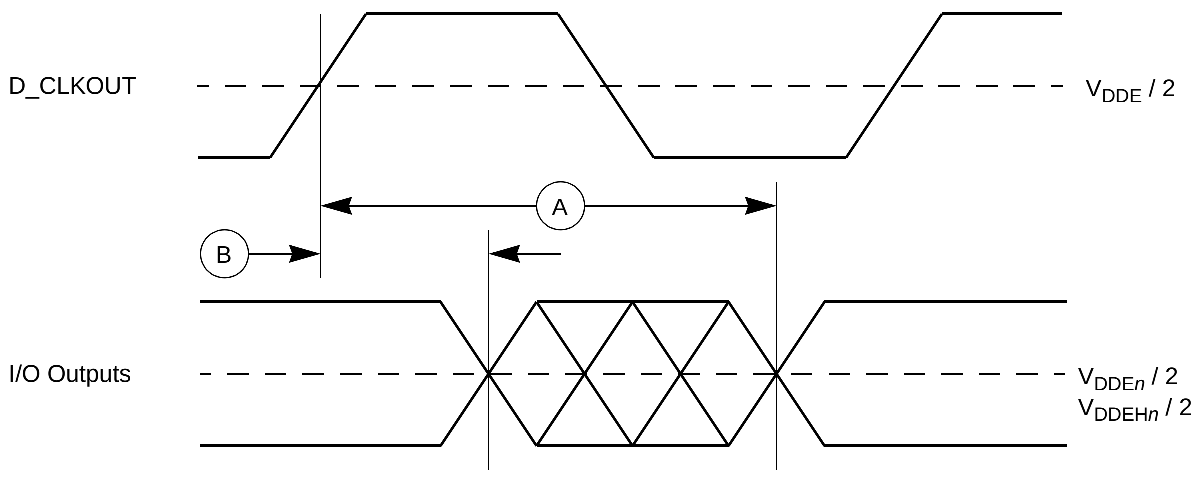


Figure 8. Generic Output Delay/Hold Timing

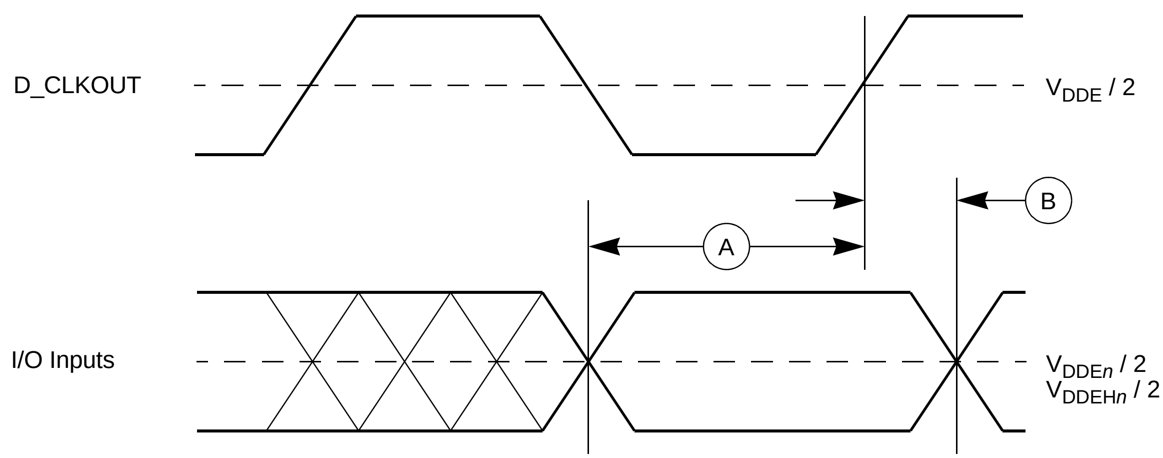


Figure 9. Generic Input Setup/Hold Timing

4.12.2 Reset and Configuration Pin Timing

Table 31. Reset and Configuration Pin Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

[1] Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, $T_A = T_L$ to T_H.

2 See Notes on t_{cyc} on Table 28.

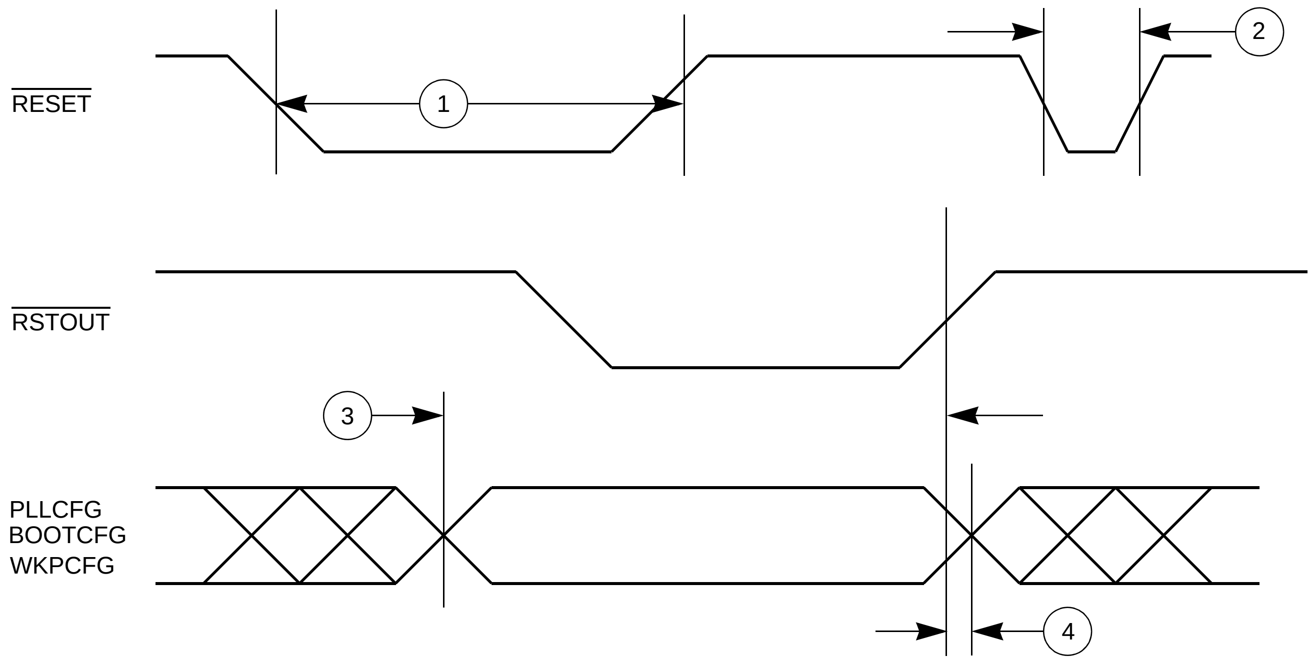


Figure 10. Reset and Configuration Pin Timing

4.12.3 IEEE 1149.1 Interface Timing

Table 32. JTAG Pin AC Electrical Characteristics[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at V_{DDE} / 2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40%–70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	10	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns

Table 32. JTAG Pin AC Electrical Characteristics[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

[1] JTAG timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 33 for functional specifications.

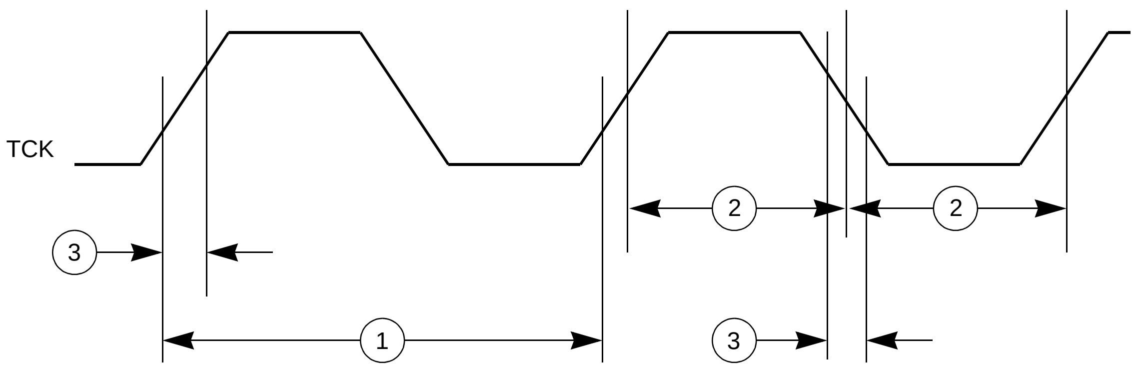


Figure 11. JTAG Test Clock Input Timing

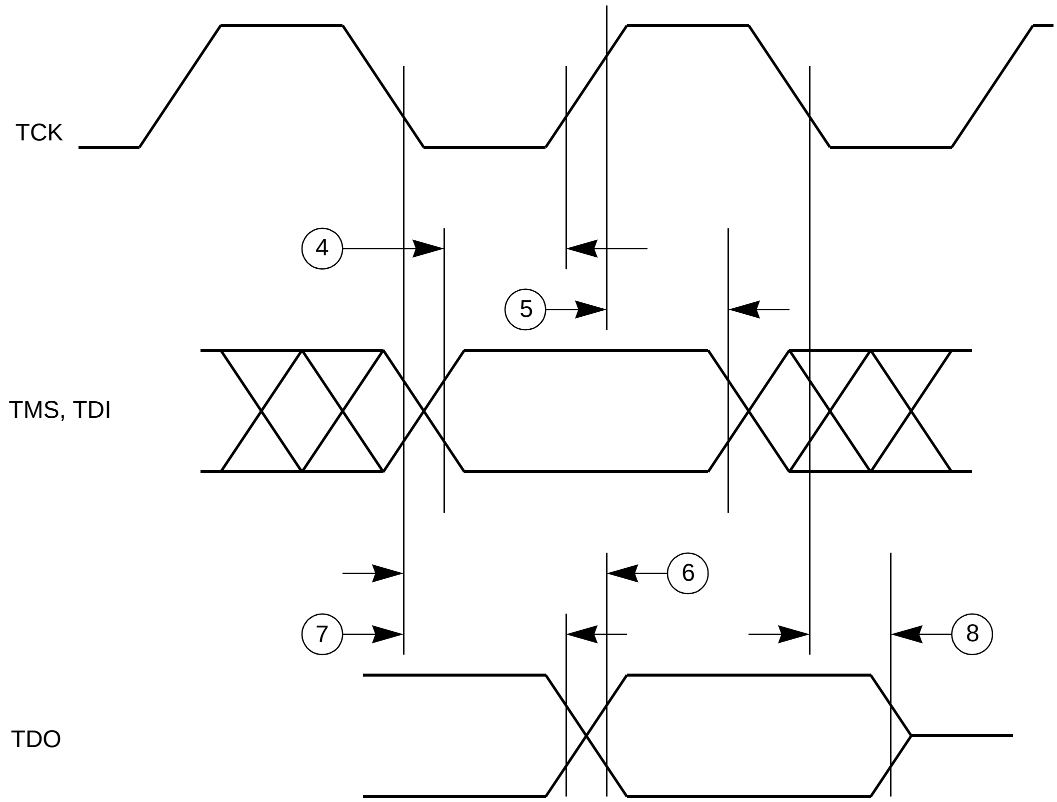


Figure 12. JTAG Test Access Port Timing

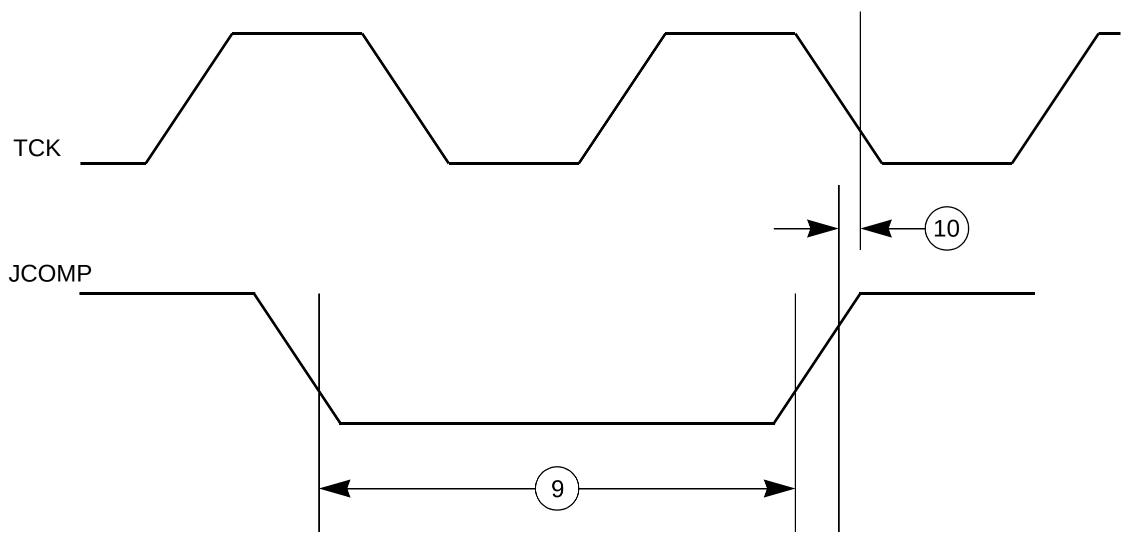


Figure 13. JTAG JCOMP Timing

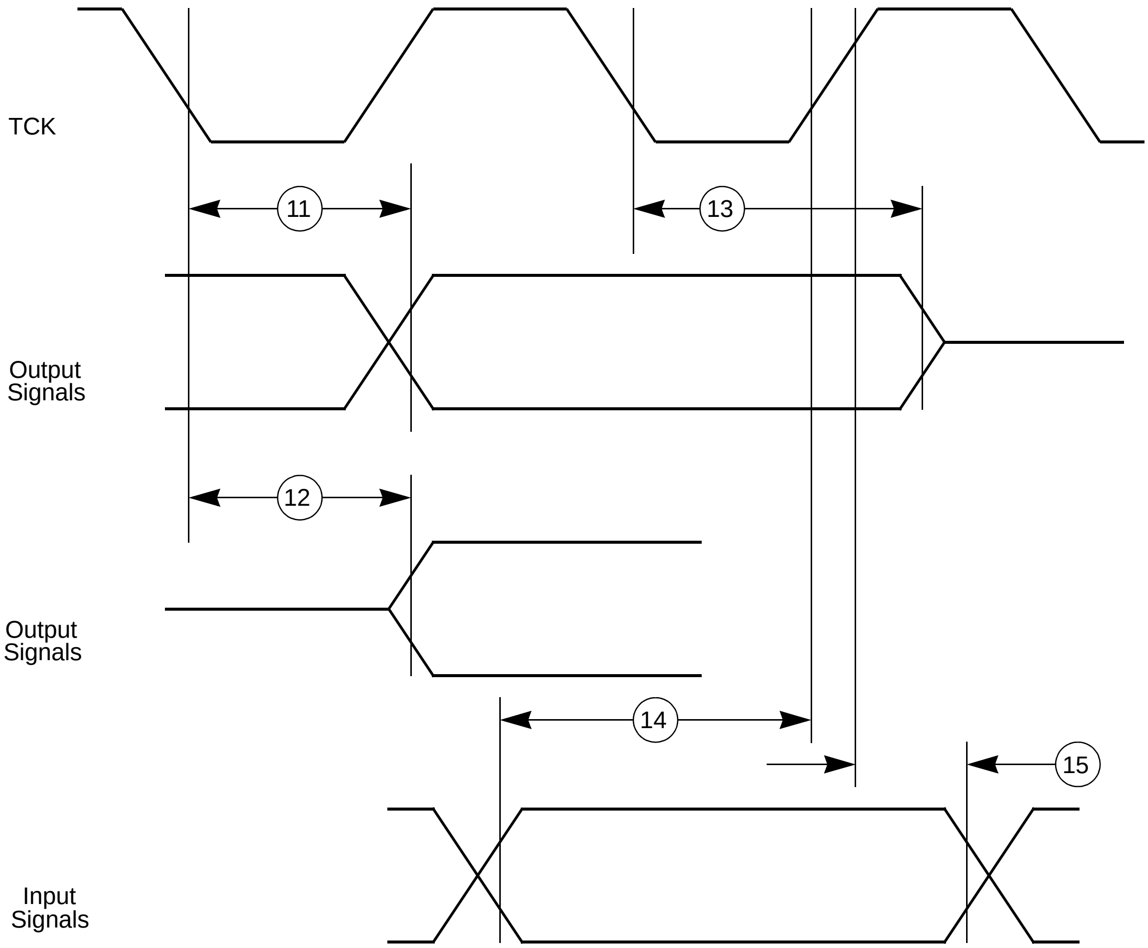


Figure 14. JTAG Boundary Scan Timing

4.12.4 Nexus Timing

Table 33. Nexus Debug Port Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2[2]	8	t_{CYC}
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[3]	t_{MDOV}	–0.1	0.2	t_{MCYC}
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[3]	t_{MSEOV}	–0.1	0.2	t_{MCYC}
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[3]	t_{EVTOV}	–0.1	0.2	t_{MCYC}
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	4[4]	—	t_{CYC}
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns

Table 33. Nexus Debug Port Timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
11	TDI, TMS Data Hold Time	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid	t_{NTDOV}	0	10	ns
13	$\overline{\text{RDY}}$ Valid to MCKO[5]	—	—	—	—
14	TDO hold time after TCLK low	t_{NTDOH}	1	—	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz (pending characterization). Set NPC_PCR[MKCO_DIV] to correct division depending on the system frequency, not to exceed maximum Nexus AUX port frequency.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

4 Lower frequency is required to be fully compliant to standard.

5 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

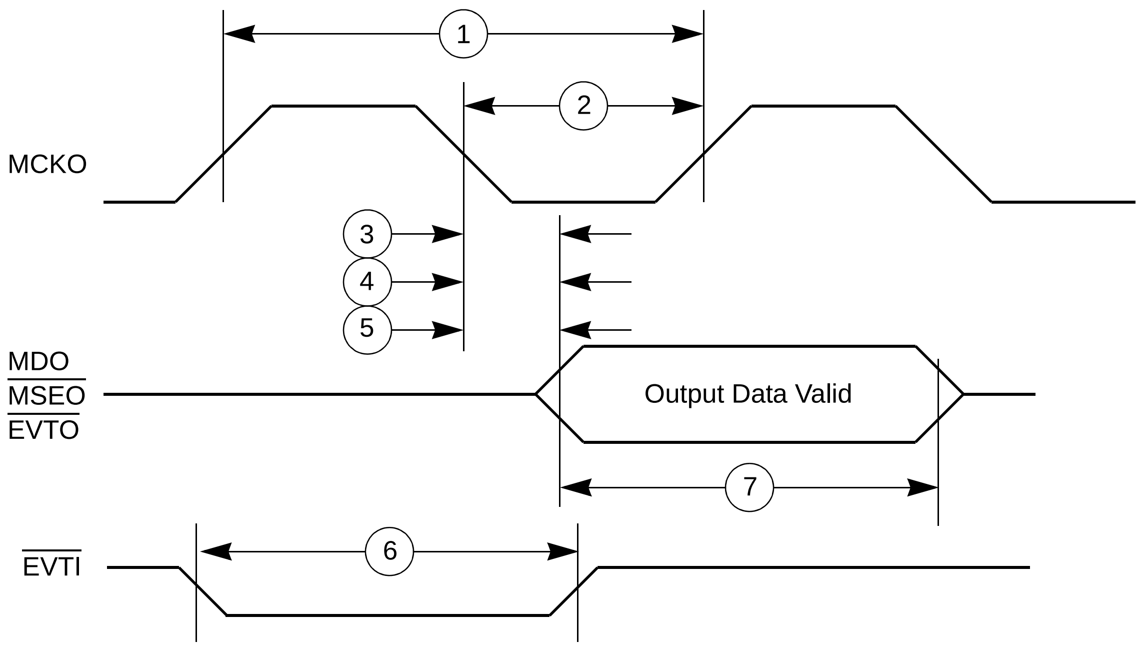


Figure 15. Nexus Timings

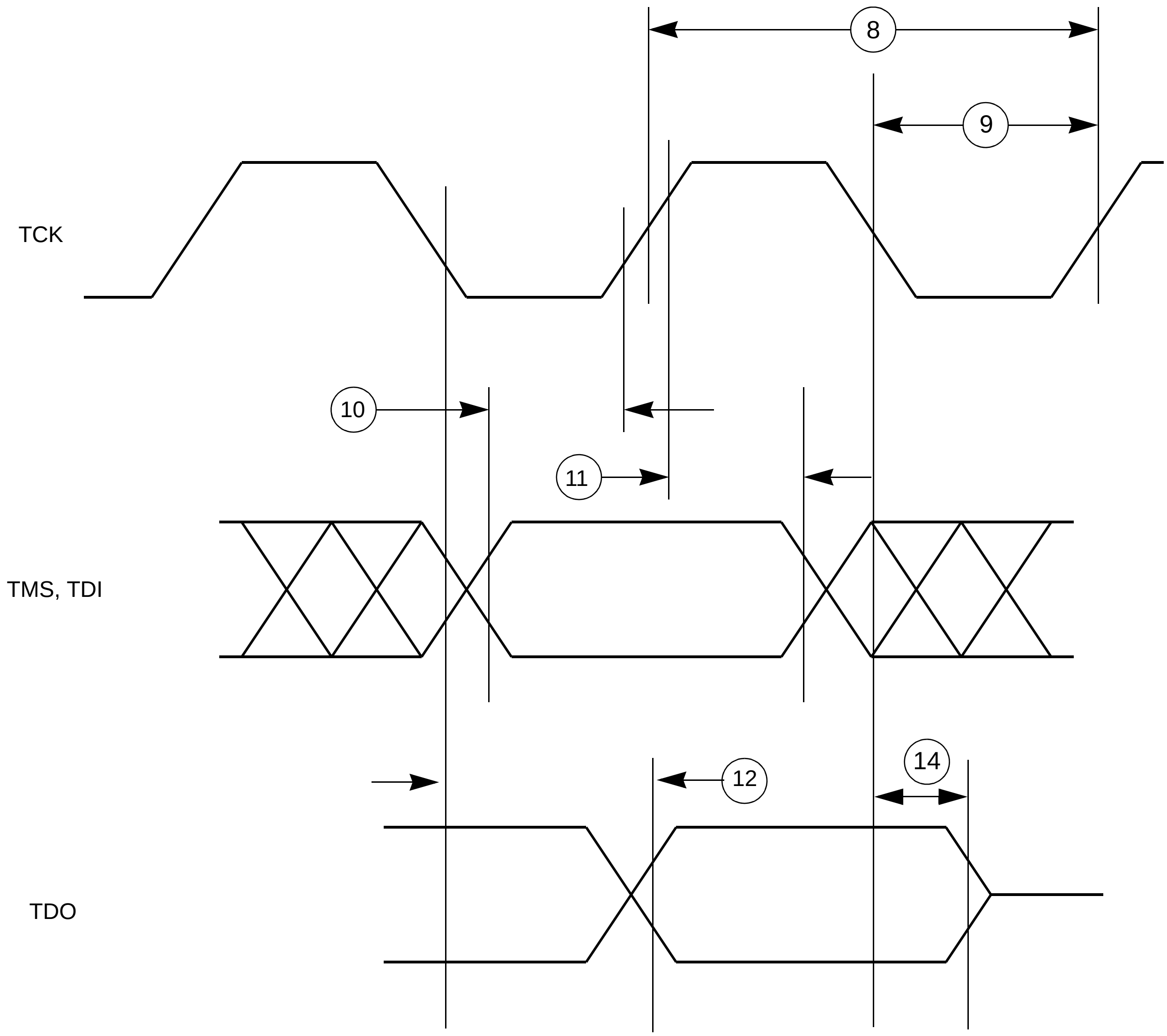


Figure 16. Nexus TCK, TDI, TMS, TDO Timing

4.12.5 External Bus Interface (EBI) Timing

Table 34. Bus Operation Timing [1]

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2 3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.

Table 34. Bus Operation Timing [1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2] [3]		Unit	Notes
			Min	Max		
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COV}	—	8.5/9.0	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 8.5 ns EBTS = 1: 9.0 ns
7	Input Signal Valid to D_CLKOUT Posedge (Setup Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIS}	5.0/4.5	—	ns	Input setup time selectable via SIU_ECCR[EBTS] bit: EBTS = 0; 5.0ns EBTS = 1; 4.5ns
8	D_CLKOUT Posedge to Input Signal Invalid (Hold Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIH}	1.0	—	ns	
9	D_ALE Pulse Width	t_{APW}	6.5	—	ns	The timing is for Asynchronous external memory system.
10	D_ALE Negated to Address Invalid	t_{AAI}	2.0/1.0 [5]	—	ns	The timing is for Asynchronous external memory system. ALE is measured at 50% of VDDE.

1 EBI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, T_A = T_L to T_H, and C_L = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM).

3 Depending on the internal bus speed, set the SIU_ECCR[EBDF] bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66 MHz.

4 Refer to Fast pad timing in Table 29 and Table 30.

5 ALE hold time spec is temperature dependant. 1.0ns spec applies for temperature range -40 to 0 C. 2.0ns spec applies to temperatures > 0 C. This spec has no dependency on SIU_ECCR[EBTS] bit.

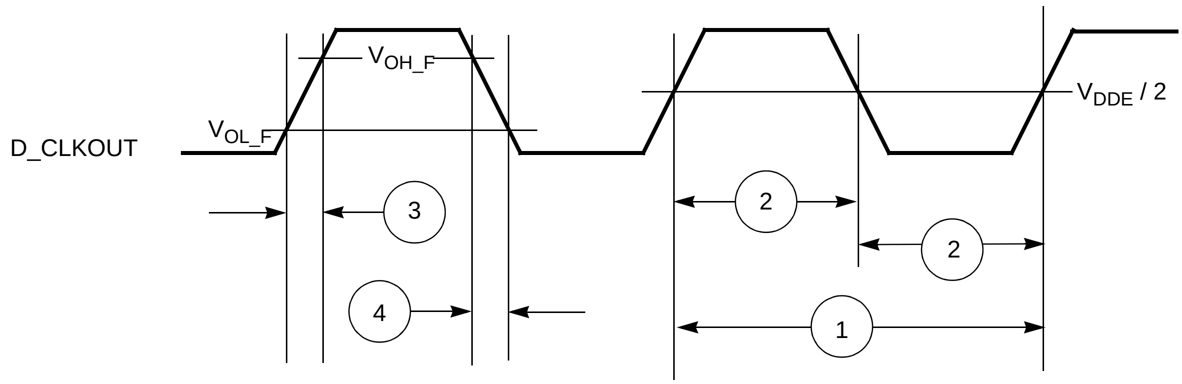


Figure 17. D_CLKOUT Timing

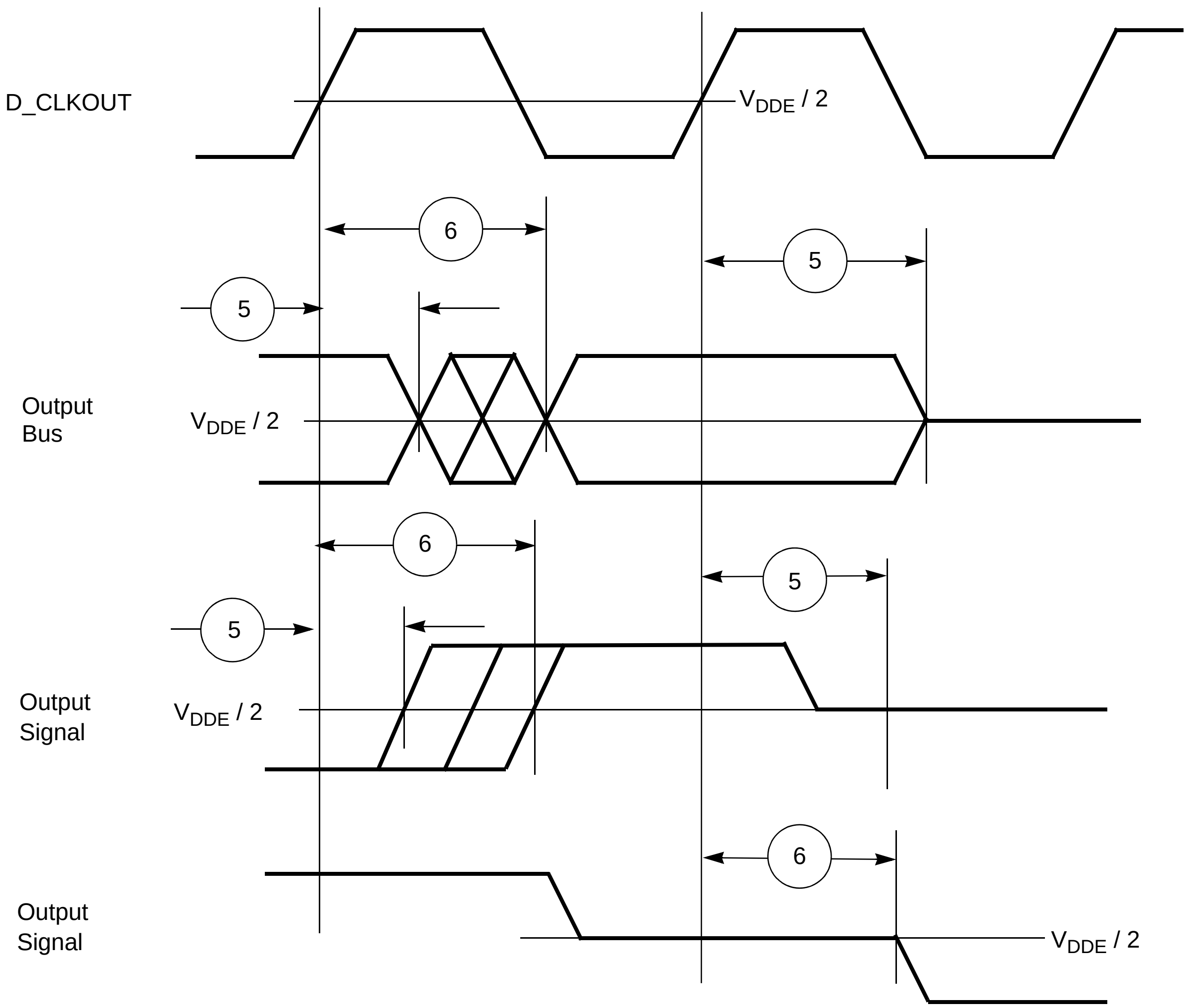


Figure 18. Synchronous Output Timing

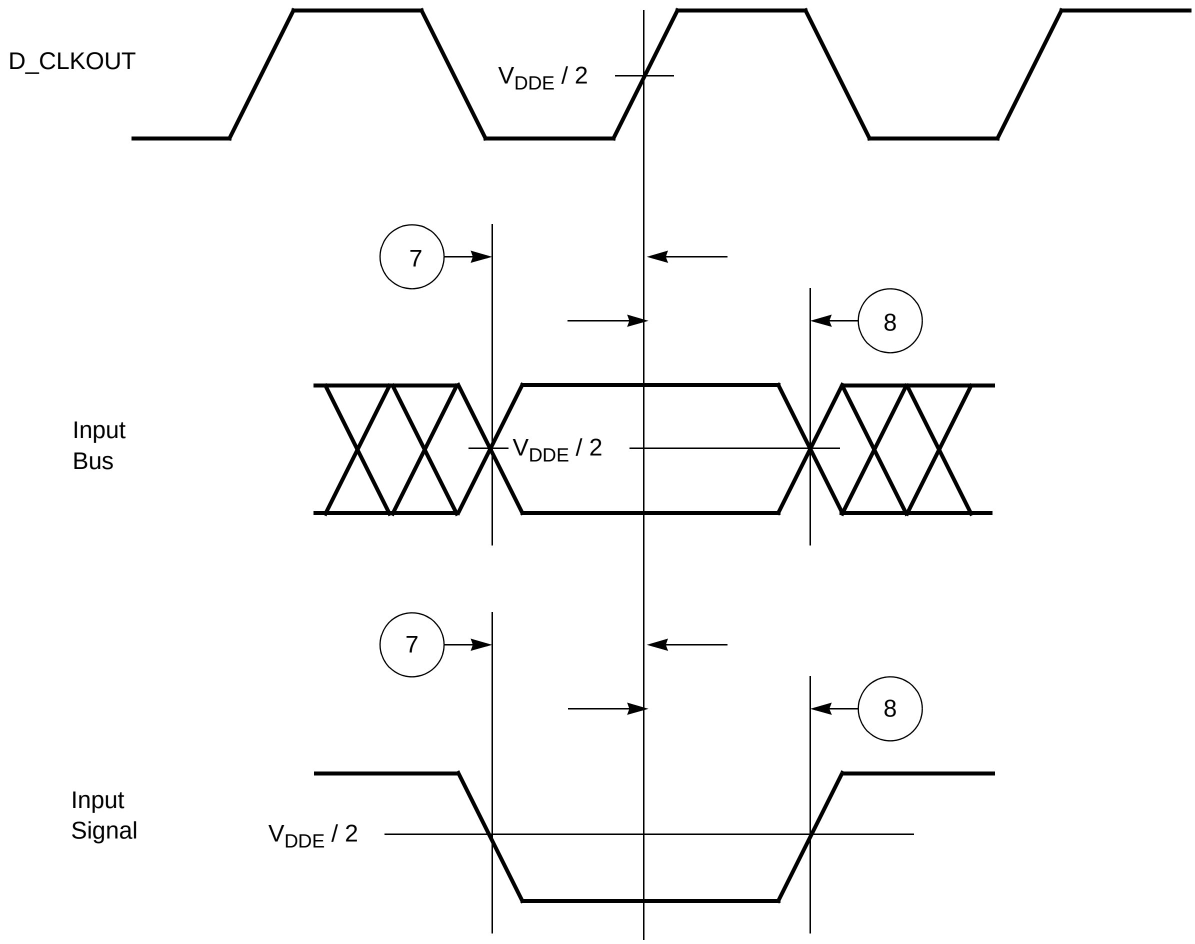


Figure 19. Synchronous Input Timing

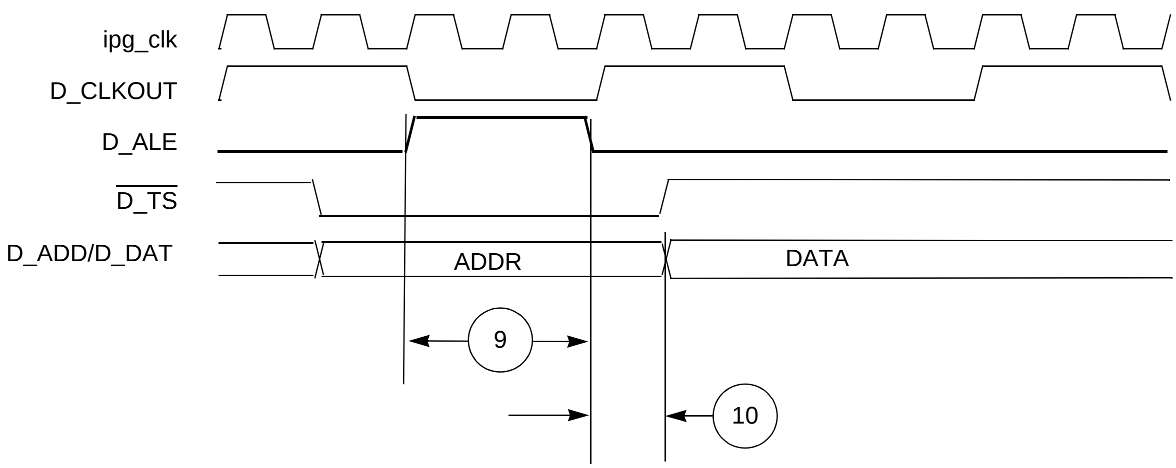


Figure 20. ALE Signal Timing

4.12.6 External Interrupt Timing (IRQ Pin)

Table 35. External Interrupt Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1 IRQ timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, T_A = T_L to T_H.

2 See Notes on t_{cyc} Table 28.

3 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

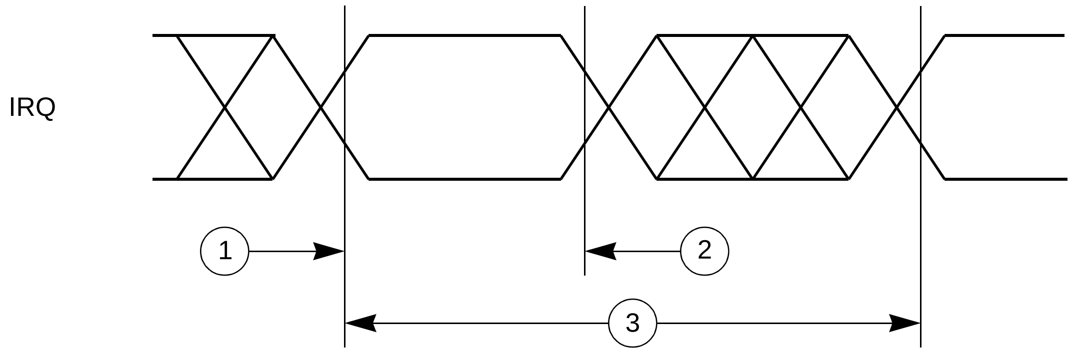


Figure 21. External Interrupt Timing

4.12.7 eTPU Timing

Table 36. eTPU Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{cyc}[2]

1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, T_A = T_L to T_H, and C_L = 200 pF with SRC = 0b00.

2 See Notes on t_{cyc} Table 28.

3 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

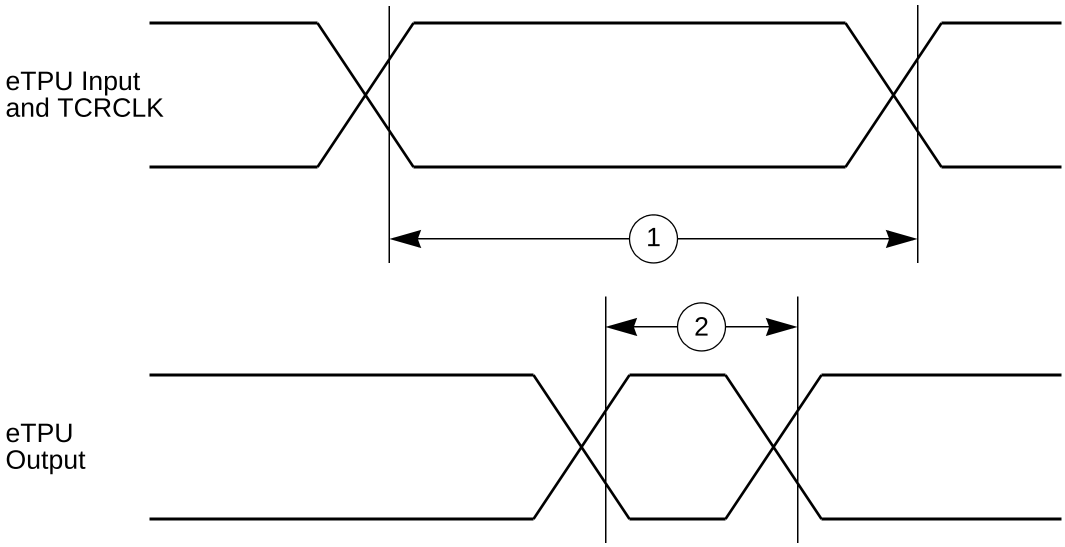


Figure 22. eTPU Timing

4.12.8 eMIOS Timing

Table 37. eMIOS Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{cyc}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{cyc}[2]

1 eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Table 28.

3 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

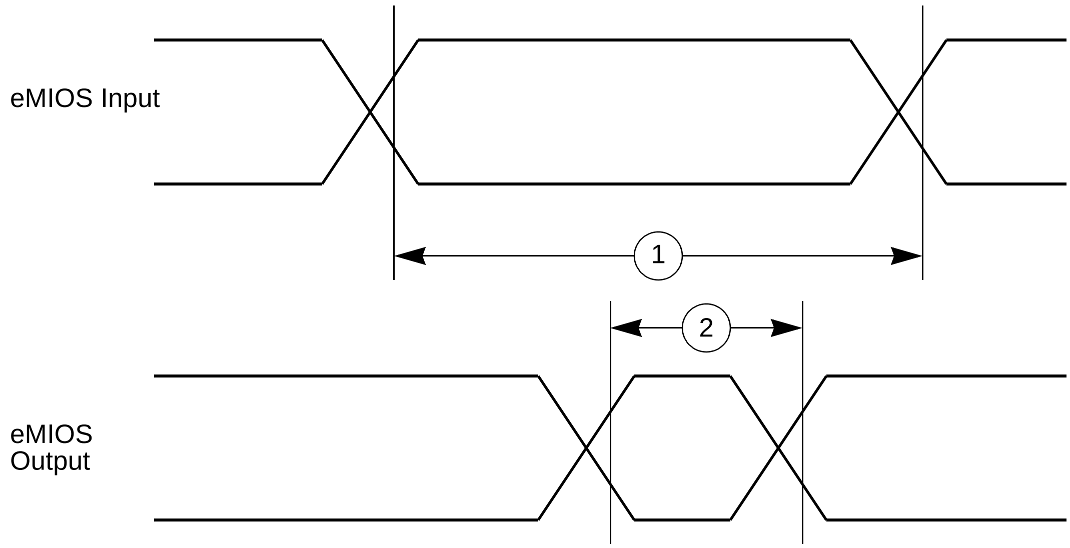


Figure 23. eMIOS Timing

4.12.9 DSPI Timing

Table 38. DSPI Timing[1,2]

Spec	Characteristic	Symbol	Peripheral Bus Freq: 92 MHz		Unit
			Min	Max	
1	DSPI Cycle Time[3, 4] Master (MTFE = 0) Slave (MTFE = 0) Master (MTFE = 1) Slave (MTFE = 1)	t_{SCK}	23.8	1800	ns
2	PCS to SCK Delay[5]	t_{CSC}	12	—	ns
3	After SCK Delay[6]	t_{ASC}	12	—	ns
4	SCK Duty Cycle	t_{SDC}	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCS*x* to $\overline{PCSS}$ time	t_{PCSC}	4	—	ns
8	$\overline{PCSS}$ to PCS*x* time	t_{PASC}	5	—	ns

Table 38. DSPI Timing[1,2] (continued)

Spec	Characteristic	Symbol	Peripheral Bus Freq: 92 MHz		Unit
			Min	Max	
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[7] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 27 10 7 27	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[7] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –3 7 12 –3	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1) Master (LVDS)	t_{SUO}	 — — — — —	 10 30 20 10 5	 ns ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1) Master (LVDS)	t_{HO}	 –6 2.5 3 –7 –5	 — — — — —	 ns ns ns ns ns

1 DSPI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, and $T_A = T_L$ to T_H

2 Speed is the nominal maximum frequency of platform clock (f_{platf}). Max speed is the maximum speed allowed including frequency modulation (FM).

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

6 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

7 This number is calculated assuming the SMPL_PT bit-field in DSPI_MCR is set to 0b10.

The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

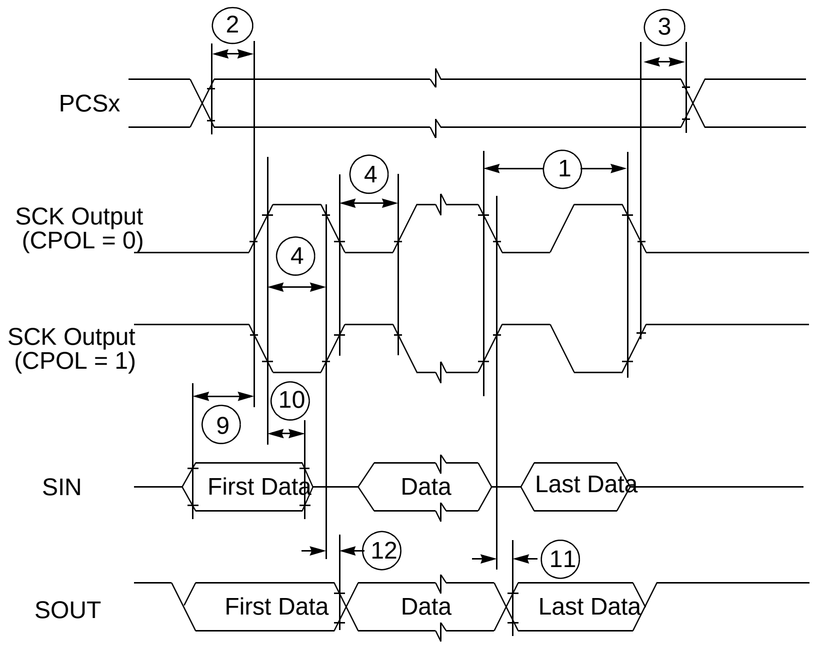


Figure 24. DSPI Classic SPI Timing — Master, CPHA = 0

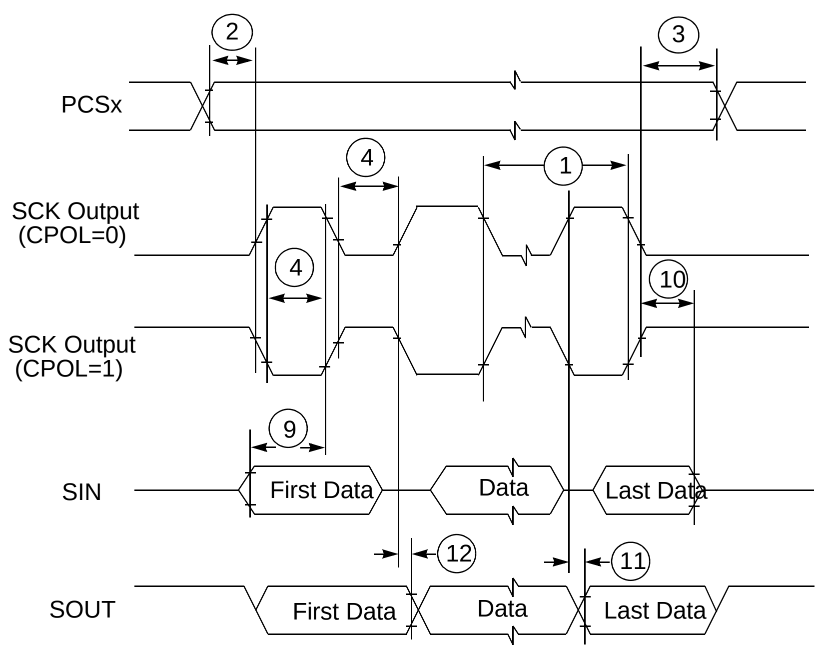


Figure 25. DSPI Classic SPI Timing — Master, CPHA = 1

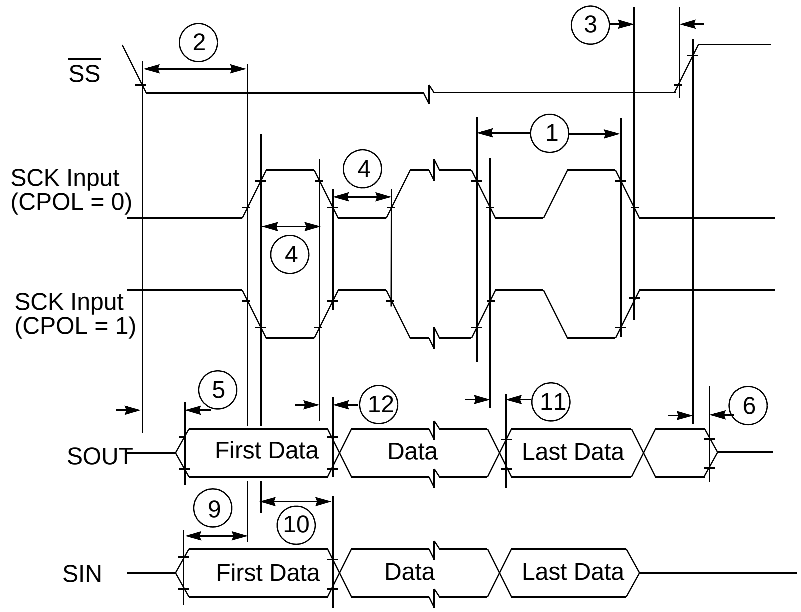


Figure 26. DSPI Classic SPI Timing — Slave, CPHA = 0

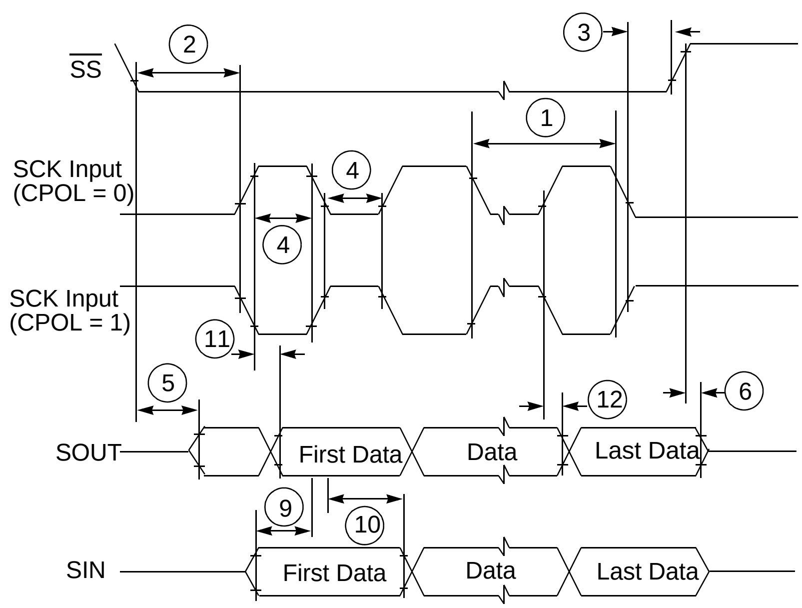


Figure 27. DSPI Classic SPI Timing — Slave, CPHA = 1

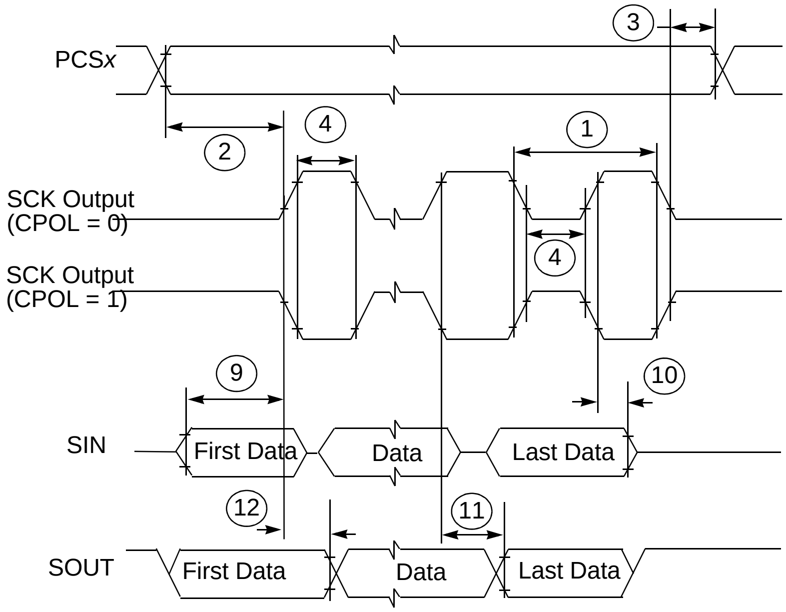


Figure 28. DSPI Modified Transfer Format Timing — Master, CPHA = 0

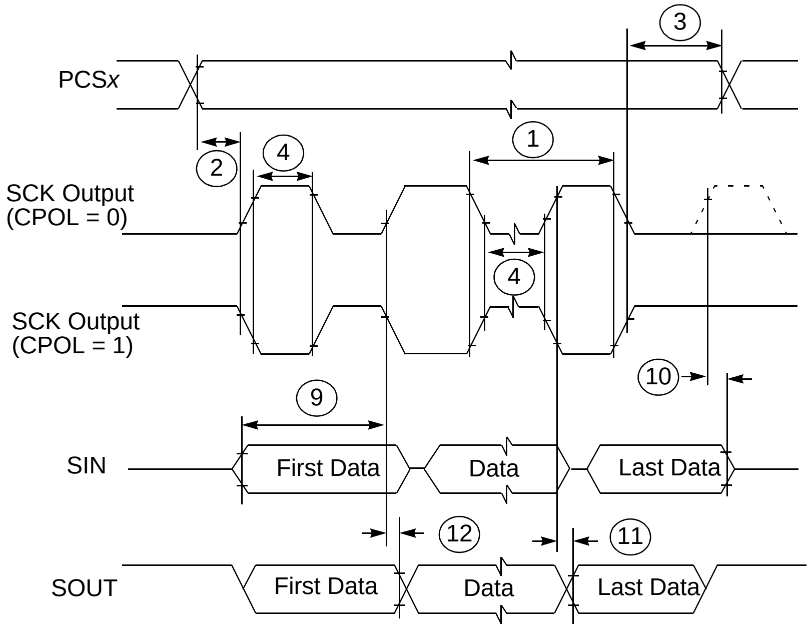


Figure 29. DSPI Modified Transfer Format Timing — Master, CPHA = 1

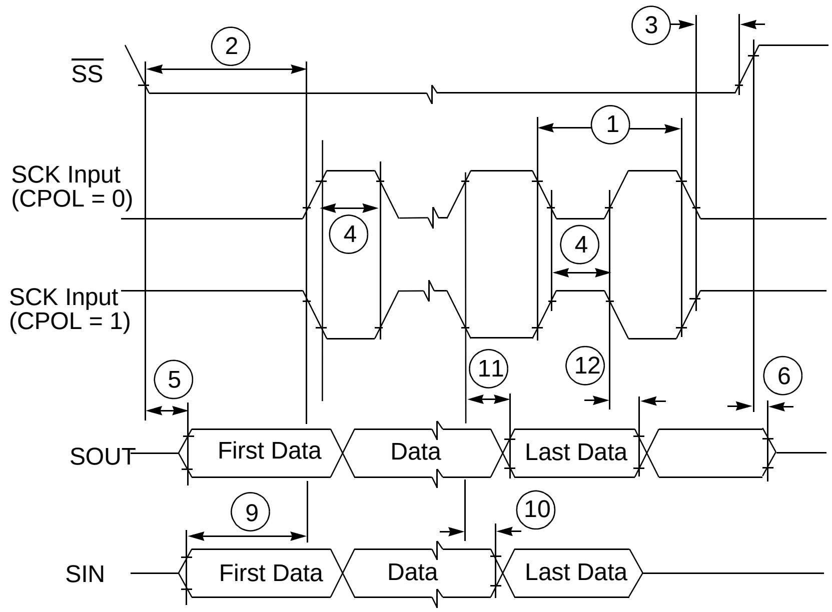


Figure 30. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

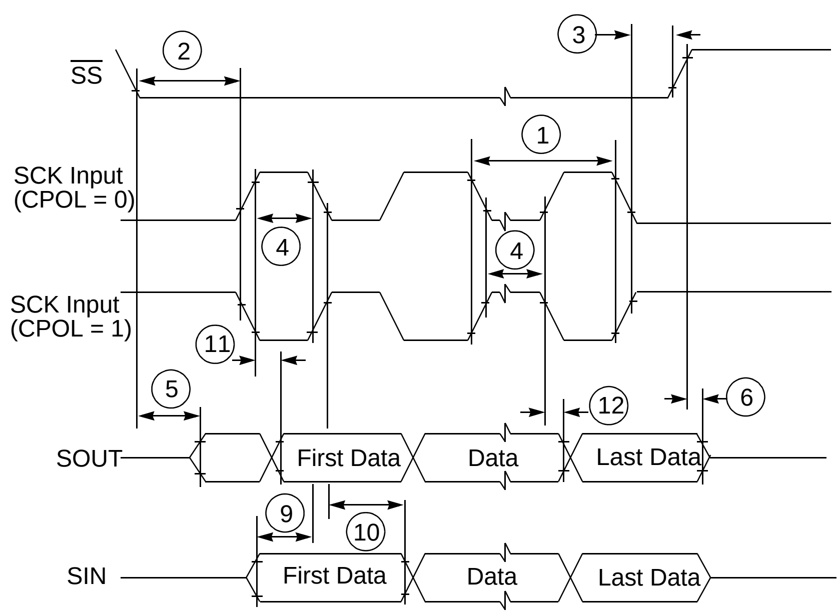


Figure 31. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

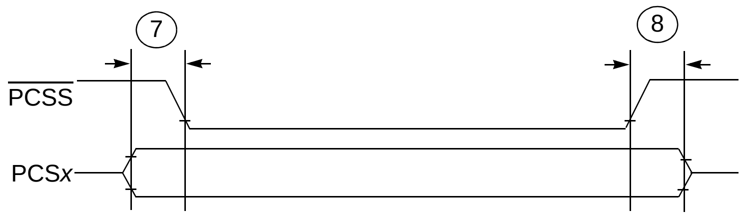


Figure 32. DSPI PCS Strobe (PCSS) Timing

5 Package Information

5.1 416-Pin Package

The package drawings of the 416-pin TEPBGA package are shown in Figure 33 and Figure 34.

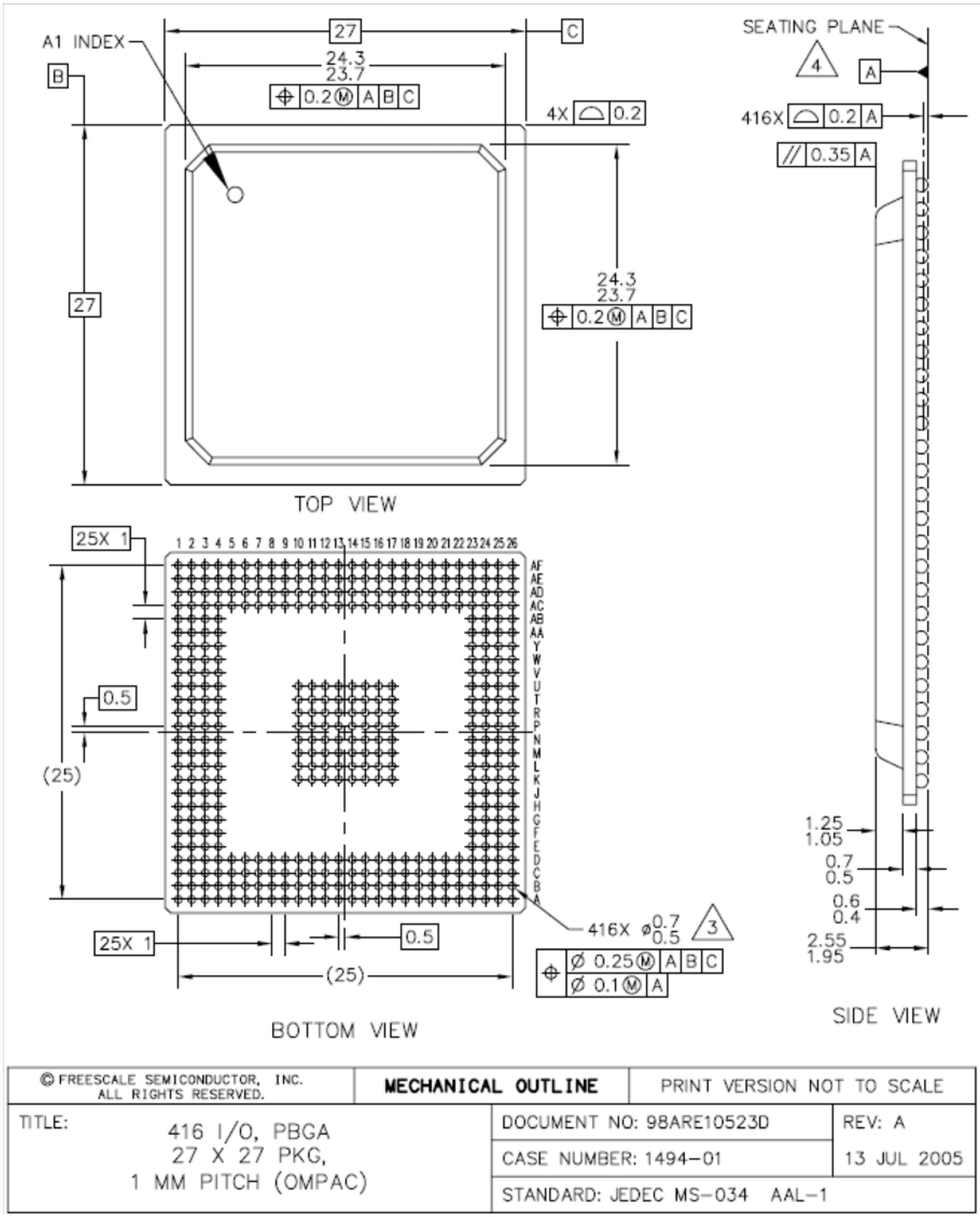


Figure 33. 416 TEPBGA Package (1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

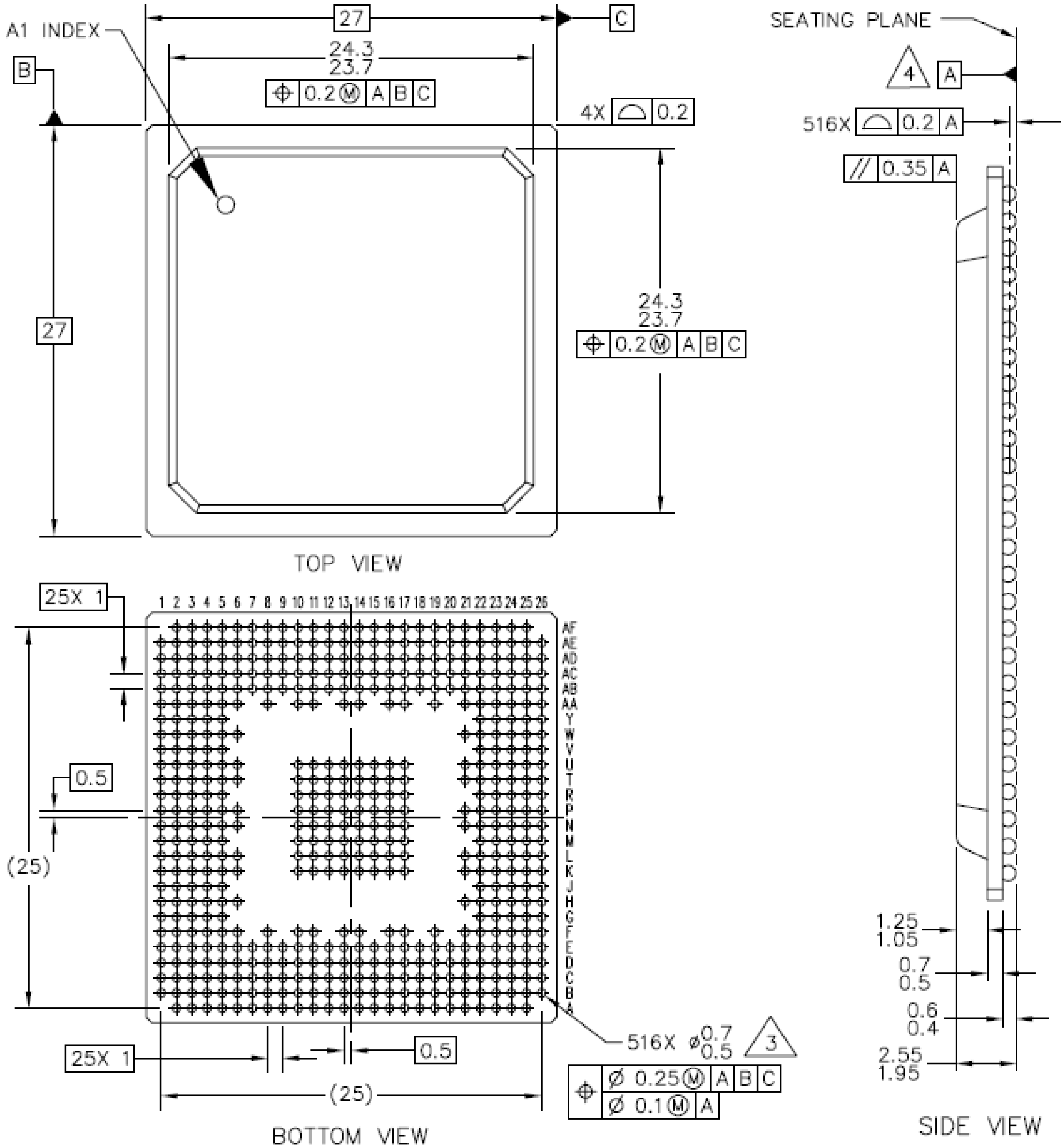
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 416 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARE10523D	REV: A	
	CASE NUMBER: 1494−01	13 JUL 2005	
	STANDARD: JEDEC MS−034 AAL−1		

Figure 34. 416 TEPBGA Package (2 of 2)

5.2 516-Pin Package

The package drawings of the 516-pin TEPBGA package are shown in Figure 35 and Figure 36.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 516 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARS10503D	REV: B
	CASE NUMBER: 1164A–01	09 AUG 2005
	STANDARD: JEDEC MS–034 AAL–1	

Figure 35. 516 TEPBGA Package (1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PACKAGE CODES: 5193 & 5198.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 516 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)		DOCUMENT NO: 98ARS10503D	REV: B
		CASE NUMBER: 1164A−01	09 AUG 2005
		STANDARD: JEDEC MS−034 AAL−1	

Figure 36. 516 TEPBGA Package (2 of 2)

6 Product Documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.nxp.com.

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

- *MPC5676R RM Microprocessor Reference Manual* (document number MPC5676RRM)

Appendix A Signal Properties and Muxing

The following table shows the signals properties for each pin on the MPC5676R. For each port pin that has an associated SIU_PCRn register to control its pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCRn[PA] bit in the order: Primary function (P), Function 2 (F2), Function 3 (F3), and GPIO (G). See Figure 37.

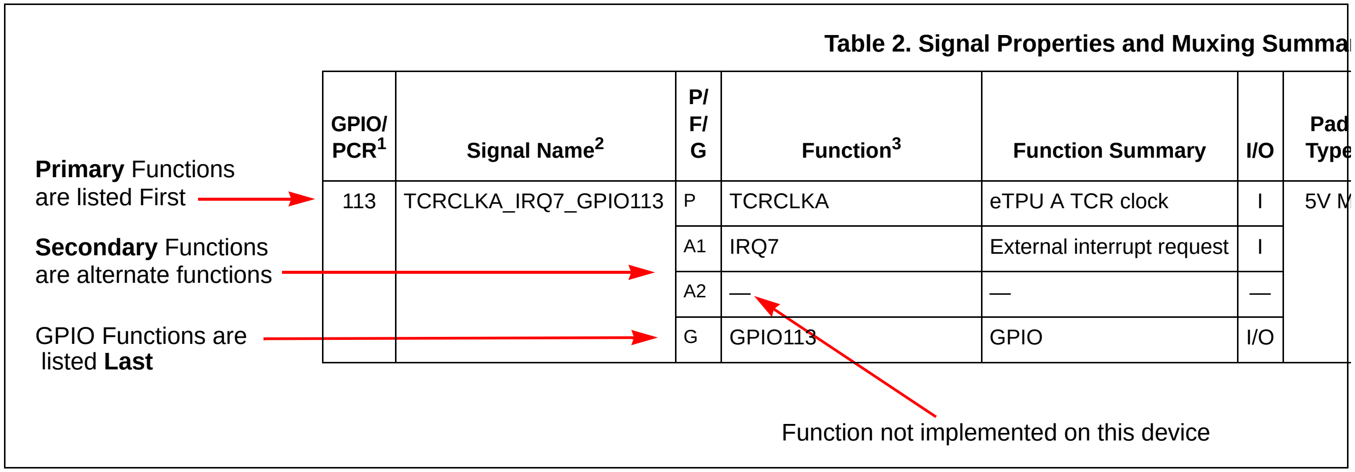


Figure 37. Supported Functions Example

Table 39. Signal Properties and Muxing Summary

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
eTPU_A											
113	TCRCLKA_IRQ7_GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up	—/Up	L1	K4
		A1	IRQ7	External interrupt request	I						
		A2	—	—	—						
		G	GPIO113	GPIO	I/O						
114	ETPUA0_ETPUA12_GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	L2	L6
		A1	ETPUA12	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO114	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	L3	J1
		A1	ETPUA13	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO115	GPIO	I/O						
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	L4	J2
		A1	ETPUA14	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO116	GPIO	I/O						
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K1	H4
		A1	ETPUA15	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO117	GPIO	I/O						
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K2	J4
		A1	ETPUA16	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO118	GPIO	I/O						
119	ETPUA5_ETPUA17_ GPIO119	P	ETPUA5	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K3	H1
		A1	ETPUA17	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO119	GPIO	I/O						
120	ETPUA6_ETPUA18_ GPIO120	P	ETPUA6	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	K4	K5
		A1	ETPUA18	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO120	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
121	ETPUA7_ETPUA19_ GPIO121	P	ETPUA7	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J1	H2
		A1	ETPUA19	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO121	GPIO	I/O						
122	ETPUA8_ETPUA20_ GPIO122	P	ETPUA8	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J2	H3
		A1	ETPUA20	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO122	GPIO	I/O						
123	ETPUA9_ETPUA21_ GPIO123	P	ETPUA9	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J3	J3
		A1	ETPUA21	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO123	GPIO	I/O						
124	ETPUA10_ETPUA22_ GPIO124	P	ETPUA10	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	J4	K6
		A1	ETPUA22	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO124	GPIO	I/O						
125	ETPUA11_ETPUA23_ GPIO125	P	ETPUA11	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H1	G1
		A1	ETPUA23	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO125	GPIO	I/O						
126	ETPUA12_PCSB1_ GPIO126	P	ETPUA12	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H2	J5
		A1	PCSB1	DSPI B peripheral chip select	O						
		A2	—	—	—						
		G	GPIO126	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
127	ETPUA13_PCSB3_ GPIO127	P	ETPUA13	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H4	G2
		A1	PCSB3	DSPI B peripheral chip select	O						
		A2	—	—	—						
		G	GPIO127	GPIO	I/O						
128	ETPUA14_PCSB4_ GPIO128	P	ETPUA14	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	H3	H5
		A1	PCSB4	DSPI B peripheral chip select	O						
		A2	—	—	—						
		G	GPIO128	GPIO	I/O						
129	ETPUA15_PCSB5_ GPIO129	P	ETPUA15	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G1	G3
		A1	PCSB5	DSPI B peripheral chip select	O						
		A2	—	—	—						
		G	GPIO129	GPIO	I/O						
130	ETPUA16_PCSD1_ GPIO130	P	ETPUA16	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G2	H6
		A1	PCSD1	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO130	GPIO	I/O						
131	ETPUA17_PCSD2_ GPIO131	P	ETPUA17	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G3	G4
		A1	PCSD2	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO131	GPIO	I/O						
132	ETPUA18_PCSD3_ GPIO132	P	ETPUA18	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	G4	G5
		A1	PCSD3	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO132	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
133	ETPUA19_PCSD4_ GPIO133	P	ETPUA19	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F1	F1
		A1	PCSD4	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO133	GPIO	I/O						
134	ETPUA20_IRQ8_ GPIO134	P	ETPUA20	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F2	F2
		A1	IRQ8	External interrupt request	I						
		A2	—	—	—						
		G	GPIO134	GPIO	I/O						
135	ETPUA21_IRQ9_ GPIO135	P	ETPUA21	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F3	F3
		A1	IRQ9	External interrupt request	I						
		A2	—	—	—						
		G	GPIO135	GPIO	I/O						
136	ETPUA22_IRQ10_ GPIO136	P	ETPUA22	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	F4	F4
		A1	IRQ10	External interrupt request	I						
		A2	—	—	—						
		G	GPIO136	GPIO	I/O						
137	ETPUA23_IRQ11_ GPIO137	P	ETPUA23	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E1	E1
		A1	IRQ11	External interrupt request	I						
		A2	—	—	—						
		G	GPIO137	GPIO	I/O						
138	ETPUA24_IRQ12_ GPIO138	P	ETPUA24	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E2	E2
		A1	IRQ12	External interrupt request	I						
		A2	—	—	—						
		G	GPIO138	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
139	ETPUA25_IRQ13_ GPIO139	P	ETPUA25	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E3	E3
		A1	IRQ13	External interrupt request	I						
		A2	—	—	—						
		G	GPIO139	GPIO	I/O						
140	ETPUA26_IRQ14_ GPIO140	P	ETPUA26	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	E4	E4
		A1	IRQ14	External interrupt request	I						
		A2	—	—	—						
		G	GPIO140	GPIO	I/O						
141	ETPUA27_IRQ15_ GPIO141	P	ETPUA27	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D1	D1
		A1	IRQ15	External interrupt request	I						
		A2	—	—	—						
		G	GPIO141	GPIO	I/O						
142	ETPUA28_PCSC1_ GPIO142	P	ETPUA28	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D2	D2
		A1	PCSC1	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO142	GPIO	I/O						
143	ETPUA29_PCSC2_ GPIO143	P	ETPUA29	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	D3	D3
		A1	PCSC2	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO143	GPIO	I/O						
144	ETPUA30_PCSC3_ GPIO144	P	ETPUA30	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C1	C1
		A1	PCSC3	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO144	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
145	ETPUA31_PCSC4_ GPIO145	P	ETPUA31	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	C2	C2
		A1	PCSC4	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO145	GPIO	I/O						
eTPU_B											
146	TCRCLKB_IRQ6_ GPIO146	P	TCRCLKB	eTPU B TCR clock	I	MH	V_{DDEH6}	—/Up	—/Up	T23	V25
		A1	IRQ6	External interrupt request	I						
		A2	—	—	—						
		G	GPIO146	GPIO	I/O						
147	ETPUB0_ETPUB16_ GPIO147	P	ETPUB0	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T24	V26
		A1	ETPUB16	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO147	GPIO	I/O						
148	ETPUB1_ETPUB17_ GPIO148	P	ETPUB1	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T25	U22
		A1	ETPUB17	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO148	GPIO	I/O						
149	ETPUB2_ETPUB18_ GPIO149	P	ETPUB2	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	T26	U23
		A1	ETPUB18	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO149	GPIO	I/O						
150	ETPUB3_ETPUB19_ GPIO150	P	ETPUB3	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R23	T22
		A1	ETPUB19	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO150	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
151	ETPUB4_ETPUB20_ GPIO151	P	ETPUB4	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R24	U24
		A1	ETPUB20	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO151	GPIO	I/O						
152	ETPUB5_ETPUB21_ GPIO152	P	ETPUB5	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R25	U25
		A1	ETPUB21	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO152	GPIO	I/O						
153	ETPUB6_ETPUB22_ GPIO153	P	ETPUB6	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	R26	U26
		A1	ETPUB22	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO153	GPIO	I/O						
154	ETPUB7_ETPUB23_ GPIO154	P	ETPUB7	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P23	T23
		A1	ETPUB23	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO154	GPIO	I/O						
155	ETPUB8_ETPUB24_ GPIO155	P	ETPUB8	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P24	T24
		A1	ETPUB24	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO155	GPIO	I/O						
156	ETPUB9_ETPUB25_ GPIO156	P	ETPUB9	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P25	R22
		A1	ETPUB25	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO156	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
157	ETPUB10_ETPUB26_ GPIO157	P	ETPUB10	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	P26	T25
		A1	ETPUB26	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO157	GPIO	I/O						
158	ETPUB11_ETPUB27_ GPIO158	P	ETPUB11	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N24	T26
		A1	ETPUB27	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO158	GPIO	I/O						
159	ETPUB12_ETPUB28_ GPIO159	P	ETPUB12	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N25	R23
		A1	ETPUB28	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO159	GPIO	I/O						
160	ETPUB13_ETPUB29_ GPIO160	P	ETPUB13	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	N26	P22
		A1	ETPUB29	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO160	GPIO	I/O						
161	ETPUB14_ETPUB30_ GPIO161	P	ETPUB14	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M25	R24
		A1	ETPUB30	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO161	GPIO	I/O						
162	ETPUB15_ETPUB31_ GPIO162	P	ETPUB15	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	M24	R25
		A1	ETPUB31	eTPU B channel (output only)	O						
		A2	—	—	—						
		G	GPIO162	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
163	ETPUB16_PCSA1_ GPIO163	P	ETPUB16	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	U26	V24
		A1	PCSA1	DSPI A peripheral chip select	O						
		A2	—	—	—						
		G	GPIO163	GPIO	I/O						
164	ETPUB17_PCSA2_ GPIO164	P	ETPUB17	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	U25	T21
		A1	PCSA2	DSPI A peripheral chip select	O						
		A2	—	—	—						
		G	GPIO164	GPIO	I/O						
165	ETPUB18_PCSA3_ GPIO165	P	ETPUB18	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	U24	W26
		A1	PCSA3	DSPI A peripheral chip select	O						
		A2	—	—	—						
		G	GPIO165	GPIO	I/O						
166	ETPUB19_PCSA4_ GPIO166	P	ETPUB19	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	U23	W25
		A1	PCSA4	DSPI A peripheral chip select	O						
		A2	—	—	—						
		G	GPIO166	GPIO	I/O						
167	ETPUB20_ GPIO167	P	ETPUB20	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	V26	W24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO167	GPIO	I/O						
168	ETPUB21_ GPIO168	P	ETPUB21	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	V25	V22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO168	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
169	ETPUB22_ GPIO169	P	ETPUB22	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	V24	V23
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO169	GPIO	I/O						
170	ETPUB23_ GPIO170	P	ETPUB23	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	W26	U21
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO170	GPIO	I/O						
171	ETPUB24_ GPIO171	P	ETPUB24	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	W25	Y25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO171	GPIO	I/O						
172	ETPUB25_ GPIO172	P	ETPUB25	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	W24	W21
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO172	GPIO	I/O						
173	ETPUB26_ GPIO173	P	ETPUB26	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	V23	Y23
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO173	GPIO	I/O						
174	ETPUB27_ GPIO174	P	ETPUB27	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	Y25	Y24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO174	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
175	ETPUB28_ GPIO175	P	ETPUB28	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	Y24	AA24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO175	GPIO	I/O						
176	ETPUB29_ GPIO176	P	ETPUB29	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	Y23	W22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO176	GPIO	I/O						
177	ETPUB30_ GPIO177	P	ETPUB30	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	AA24	AB24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO177	GPIO	I/O						
178	ETPUB31_ GPIO178	P	ETPUB31	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG	—/WKPCFG	AB24	Y22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO178	GPIO	I/O						
eTPU_C											
440	TCRCLKC_ GPIO440	P	TCRCLKC	eTPU C TCR clock	I	MH	V_{DDEH7}	—/Up	—/Up	B26	F22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO440	GPIO	I/O						
441	ETPUC0_ GPIO441	P	ETPUC0	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	C25	C25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO441	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
442	ETPUC1_ GPIO442	P	ETPUC1	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	C26	C26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO442	GPIO	I/O						
443	ETPUC2_ GPIO443	P	ETPUC2	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	D25	D25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO443	GPIO	I/O						
444	ETPUC3_ GPIO444	P	ETPUC3	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	D26	D26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO444	GPIO	I/O						
445	ETPUC4_ PCSE1_GPIO445	P	ETPUC4	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E24	E24
		A1		DSPI E peripheral chip select							
		A2	—	—	—						
		G	GPIO445	GPIO	I/O						
446	ETPUC5_ PCSE2_GPIO446	P	ETPUC5	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E25	E25
		A1		DSPI E peripheral chip select							
		A2	—	—	—						
		G	GPIO446	GPIO	I/O						
447	ETPUC6_ PCSE3_GPIO447	P	ETPUC6	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	E26	E26
		A1		DSPI E peripheral chip select							
		A2	—	—	—						
		G	GPIO447	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
448	ETPUC7_ PCSE4_GPIO448	P	ETPUC7	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F23	F23
		A1		DSPI E peripheral chip select							
		A2	—	—	—						
		G	GPIO448	GPIO	I/O						
449	ETPUC8_ PCSE5_GPIO449	P	ETPUC8	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F24	F24
		A1		DSPI E peripheral chip select							
		A2	—	—	—						
		G	GPIO449	GPIO	I/O						
450	ETPUC9_IRQ0_ GPIO450	P	ETPUC9	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F25	F25
		A1	IRQ0	External interrupt request	I						
		A2	—	—	—						
		G	GPIO450	GPIO	I/O						
451	ETPUC10__IRQ1_ GPIO451	P	ETPUC10	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	F26	F26
		A1	IRQ1	External interrupt request	I						
		A2	—	—	—						
		G	GPIO451	GPIO	I/O						
452	ETPUC11_IRQ2_ GPIO452	P	ETPUC11	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G23	G22
		A1	IRQ2	External interrupt request	I						
		A2	—	—	—						
		G	GPIO452	GPIO	I/O						
453	ETPUC12_IRQ3_ GPIO453	P	ETPUC12	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G24	G23
		A1	IRQ3	External interrupt request	I						
		A2	—	—	—						
		G	GPIO453	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
454	ETPUC13_3_IRQ4_ GPIO454	P	ETPUC13	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G25	G24
		A1	IRQ4	External interrupt request	I						
		A2	—	—	—						
		G	GPIO454	GPIO	I/O						
455	ETPUC14_4_IRQ5_ GPIO455	P	ETPUC14	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	G26	G25
		A1	IRQ5	External interrupt request	I						
		A2	—	—	—						
		G	GPIO455	GPIO	I/O						
456	ETPUC15__ GPIO456	P	ETPUC15	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H23	G26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO456	GPIO	I/O						
457	ETPUC16_FR_A_TX_ GPIO457	P	ETPUC16	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H24	H22
		A1	FR_A_TX	FlexRay A transfer	O						
		A2	—	—	—						
		G	GPIO457	GPIO	I/O						
458	ETPUC17_FR_A_RX_ GPIO458	P	ETPUC17	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H25	H23
		A1	FR_A_RX	FlexRay A receive	I						
		A2	—	—	—						
		G	GPIO458	GPIO	I/O						
459	ETPUC18_FR_A_TX_EN_ GPIO459	P	ETPUC18	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	H26	H24
		A1	FR_A_TX_EN	FlexRay A transfer enable	O						
		A2	—	—	—						
		G	GPIO459	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
460	ETPUC19_TXDA_ GPIO460	P	ETPUC19	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J23	H21
		A1	TXDA	eSCI A transmit	O						
		A2	—	—	—						
		G	GPIO460	GPIO	I/O						
461	ETPUC20_RXDA _ GPIO461	P	ETPUC20	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J24	H25
		A1	RXDA	eSCI A receive	I						
		A2	—	—	—						
		G	GPIO461	GPIO	I/O						
462	ETPUC21_TXDB_ GPIO462	P	ETPUC21	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J25	H26
		A1	TXDB	eSCI B transmit	O						
		A2	—	—	—						
		G	GPIO462	GPIO	I/O						
463	ETPUC22_RXDB_ GPIO463	P	ETPUC22	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	J26	J22
		A1	RXDB	eSCI B receive	I						
		A2	—	—	—						
		G	GPIO463	GPIO	I/O						
464	ETPUC23_PCSD5_ GPIO464	P	ETPUC23	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K23	J23
		A1	PCSD5	DSPI D peripheral chip select	O						
		A2	MAA0	ADC A Mux Address 0	O						
		A3	MAB0	ADC B Mux Address 0	O						
		G	GPIO464	GPIO	I/O						
465	ETPUC24_PCSD4_ GPIO465	P	ETPUC24	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K24	J24
		A1	PCSD4	DSPI D peripheral chip select	O						
		A2	MAA1	ADC A Mux Address 1	O						
		A4	MAB1	ADC B Mux Address 1	O						
		G	GPIO465	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
466	ETPUC25_PCSD3_ GPIO466	P	ETPUC25	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K25	K21
		A1	PCSD3	DSPI D peripheral chip select	O						
		A2	MAA2	ADC A Mux Address 2	O						
		A3	MAB2	ADC B Mux Address 2	O						
		G	GPIO466	GPIO	I/O						
467	ETPUC26_PCSD2_ GPIO467	P	ETPUC26	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	K26	J25
		A1	PCSD2	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO467	GPIO	I/O						
468	ETPUC27_PCSD1_ GPIO468	P	ETPUC27	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L23	J26
		A1	PCSD1	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO468	GPIO	I/O						
469	ETPUC28_PCSD0_ GPIO469	P	ETPUC28	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L24	K22
		A1	PCSD0	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO469	GPIO	I/O						
470	ETPUC29_SCKD_ GPIO470	P	ETPUC29	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L25	K23
		A1	SCKD	DSPI D clock	I/O						
		A2	—	—	—						
		G	GPIO470	GPIO	I/O						
471	ETPUC30_SOUTD_ GPIO471	P	ETPUC30	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	L26	K24
		A1	SOUTD	DSPI D data output	O						
		A2	—	—	—						
		G	GPIO471	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
472	ETPUC31_SIND_ GPIO472	P	ETPUC31	eTPU C channel	I/O	MH	V_{DDEH7}	—/WKPCFG	—/WKPCFG	M23	K25
		A1	SIND	DSPI D data input	I						
		A2	—	—	—						
		G	GPIO472	GPIO	I/O						
eMIOS											
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE10	AC13
		A1	ETPUA0	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO179	GPIO	I/O						
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF10	AB13
		A1	ETPUA1	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO180	GPIO	I/O						
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD11	AD13
		A1	ETPUA2	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO181	GPIO	I/O						
182	EMIOS3_ETPUA3_ GPIO182	P	EMIOS3	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE11	AE13
		A1	ETPUA3	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO182	GPIO	I/O						
183	EMIOS4_ETPUA4_ GPIO183	P	EMIOS4	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF11	AF13
		A1	ETPUA4	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO183	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
184	EMIOS5_ETPUA5_ GPIO184	P	EMIOS5	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD12	AF14
		A1	ETPUA5	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO184	GPIO	I/O						
185	EMIOS6_ETPUA6_ GPIO185	P	EMIOS6	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE12	AE14
		A1	ETPUA6	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO185	GPIO	I/O						
186	EMIOS7_ETPUA7_ GPIO186	P	EMIOS7	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF12	AD14
		A1	ETPUA7	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO186	GPIO	I/O						
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC13	AC14
		A1	ETPUA8	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO187	GPIO	I/O						
188	EMIOS9_ETPUA9_ GPIO188	P	EMIOS9	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD13	AF15
		A1	ETPUA9	eTPU A channel	O						
		A2	—	—	—						
		G	GPIO188	GPIO	I/O						
189	EMIOS10_SCKD_ GPIO189	P	EMIOS10	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE13	AE15
		A1	SCKD	DSPI D clock	O						
		A2	—	—	—						
		G	GPIO189	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
190	EMIOS11_SIND_ GPIO190	P	EMIOS11	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF13	AB14
		A1	SIND	DSPI D data input	I						
		A2	—	—	—						
		G	GPIO190	GPIO	I/O						
191	EMIOS12_SOUTC_ GPIO191	P	EMIOS12	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF14	AD15
		A1	SOUTC	DSPI C data output	O						
		A2	—	—	—						
		G	GPIO191	GPIO	I/O						
192	EMIOS13_SOUTD_ GPIO192	P	EMIOS13	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE14	AC15
		A1	SOUTD	DSPI D data output	O						
		A2	—	—	—						
		G	GPIO192	GPIO	I/O						
193	EMIOS14_IRQ0_ GPIO193	P	EMIOS14	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC14	AF17
		A1	IRQ0	External interrupt request	I						
		A2	CNTXD	FlexCAN D transmit	O						
		G	GPIO193	GPIO	I/O						
194	EMIOS15_IRQ1_ GPIO194	P	EMIOS15	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD14	AE16
		A1	IRQ1	External interrupt request	I						
		A2	CNRXD	FlexCAN D receive	I						
		G	GPIO194	GPIO	I/O						
195	EMIOS16_ETPUB0_ GPIO195	P	EMIOS16	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF15	AD16
		A1	ETPUB0	eTPU B channel	O						
		A2	FR_DBG[3]	FlexRay debug	O						
		G	GPIO195	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
196	EMIOS17_ETPUB1_ GPIO196	P	EMIOS17	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE15	AB15
		A1	ETPUB1	eTPU B channel	O						
		A2	FR_DBG[2]	FlexRay debug	O						
		G	GPIO196	GPIO	I/O						
197	EMIOS18_ETPUB2_ GPIO197	P	EMIOS18	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC15	AD17
		A1	ETPUB2	eTPU B channel	O						
		A2	FR_DBG[1]	FlexRay debug	O						
		G	GPIO197	GPIO	I/O						
198	EMIOS19_ETPUB3_ GPIO198	P	EMIOS19	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD15	AB16
		A1	ETPUB3	eTPU B channel	O						
		A2	FR_DBG[0]	FlexRay debug	O						
		G	GPIO198	GPIO	I/O						
199	EMIOS20_ETPUB4_ GPIO199	P	EMIOS20	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF16	AF16
		A1	ETPUB4	eTPU B channel	O						
		A2	—	—	—						
		G	GPIO199	GPIO	I/O						
200	EMIOS21_ETPUB5_ GPIO200	P	EMIOS21	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE16	AE17
		A1	ETPUB5	eTPU B channel	O						
		A2	—	—	—						
		G	GPIO200	GPIO	I/O						
201	EMIOS22_ETPUB6_ GPIO201	P	EMIOS22	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC16	AC16
		A1	ETPUB6	eTPU B channel	O						
		A2	—	—	—						
		G	GPIO201	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
202	EMIOS23_ETPUB7_ GPIO202	P	EMIOS23	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD16	AA16
		A1	ETPUB7	eTPU B channel	O						
		A2	—	—	—						
		G	GPIO202	GPIO	I/O						
203	EMIOS24_PCSB0_ GPIO203	P	EMIOS24	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF17	AC17
		A1	PCSB0	DSPI B peripheral chip select	I/O						
		A2	—	—	—						
		G	GPIO203	GPIO	I/O						
204	EMIOS25_PCSB1_ GPIO204	P	EMIOS25	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE17	AF18
		A1	PCSB1	DSPI B peripheral chip select	O						
		A2	—	—	—						
		G	GPIO204	GPIO	I/O						
432	EMIOS26_PCSB2_ GPIO432	P	EMIOS26	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD17	AE18
		A1	PCSB2	DSPI B peripheral chip select	O						
		A2	—	—	—						
		G	GPIO432	GPIO	I/O						
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC17	AD18
		A1	PCSB3	DSPI B peripheral chip select	O						
		A2	—	—	—						
		G	GPIO433	GPIO	I/O						
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AF18	AC18
		A1	PCSC0	DSPI C peripheral chip select	I/O						
		A2	—	—	—						
		G	GPIO434	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AE18	AB17
		A1	PCSC1	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO435	GPIO	I/O						
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AD18	AF19
		A1	PCSC2	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO436	GPIO	I/O						
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG	—/WKPCFG	AC18	AA17
		A1	PCSC5	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO437	GPIO	I/O						
eQADC											
—	ANA0	P	ANA0[9]	eQADC A shared analog input	I	AE/up-down	V_{DDA_A1}	ANA0	ANA0	A4	A4
—	ANA1	P	ANA1[9]	eQADC A shared analog input	I	AE/up-down	V_{DDA_A1}	ANA1	ANA1	B5	B5
—	ANA2	P	ANA2[9]	eQADC A shared analog input	I	AE/up-down	V_{DDA_A1}	ANA2	ANA2	C5	C5
—	ANA3	P	ANA3[9]	eQADC A shared analog input	I	AE/up-down	V_{DDA_A1}	ANA3	ANA3	D6	D6
—	ANA4	P	ANA4[9]	eQADC A shared analog input	I	AE/up-down	V_{DDA_A1}	ANA4	ANA4	A5	A5
—	ANA5	P	ANA5[9]	eQADC A shared analog input	I	AE/up-down	V_{DDA_A1}	ANA5	ANA5	B6	B6
—	ANA6	P	ANA6[9]	eQADC A shared analog input	I	AE/up-down	V_{DDA_A1}	ANA6	ANA6	C6	C6
—	ANA7	P	ANA7[9]	eQADC A shared analog input	I	AE/up-down	V_{DDA_A1}	ANA7	ANA7	D7	C7

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
—	ANA8	P	ANA8	eQADC A analog input	I	AE	V_{DDA_A1}	ANA8	ANA8	A6	D7
—	ANA9	P	ANA9	eQADC A analog input	I	AE	V_{DDA_A1}	ANA9	ANA9	C7	A6
—	ANA10	P	ANA10	eQADC A analog input	I	AE	V_{DDA_A1}	ANA10	ANA10	B7	B7
—	ANA11	P	ANA11	eQADC A analog input	I	AE	V_{DDA_A1}	ANA11	ANA11	A7	A7
—	ANA12	P	ANA12	eQADC A analog input	I	AE	V_{DDA_A1}	ANA12	ANA12	D8	D8
—	ANA13	P	ANA13	eQADC A analog input	I	AE	V_{DDA_A1}	ANA13	ANA13	C8	C8
—	ANA14	P	ANA14	eQADC A analog input	I	AE	V_{DDA_A1}	ANA14	ANA14	B8	B8
—	ANA15	P	ANA15	eQADC A analog input	I	AE	V_{DDA_A1}	ANA15	ANA15	A8	A8
—	ANA16	P	ANA16	eQADC A analog input	I	AE	V_{DDA_A1}	ANA16	ANA16	D9	D9
—	ANA17	P	ANA17	eQADC A analog input	I	AE	V_{DDA_A1}	ANA17	ANA17	C9	C9
—	ANA18	P	ANA18	eQADC A analog input	I	AE	V_{DDA_A1}	ANA18	ANA18	D10	D10
—	ANA19	P	ANA19	eQADC A analog input	I	AE	V_{DDA_A1}	ANA19	ANA19	C10	C10
—	ANA20	P	ANA20	eQADC A analog input	I	AE	V_{DDA_A1}	ANA20	ANA20	D11	D11
—	ANA21	P	ANA21	eQADC A analog input	I	AE	V_{DDA_A1}	ANA21	ANA21	C11	C11
—	ANA22	P	ANA22	eQADC A analog input	I	AE	V_{DDA_A1}	ANA22	ANA22	D12	C12
—	ANA23	P	ANA23	eQADC A analog input	I	AE	V_{DDA_A1}	ANA23	ANA23	C12	D12
—	AN24	P	AN24	eQADC analog input	I	AE	V_{DDA_A0}	AN24	AN24	B12	B12
—	AN25	P	AN25	eQADC analog input	I	AE	V_{DDA_A0}	AN25	AN25	D13	C13
—	AN26	P	AN26	eQADC analog input	I	AE	V_{DDA_A0}	AN26	AN26	C13	D13
—	AN27	P	AN27	eQADC analog input	I	AE	V_{DDA_A0}	AN27	AN27	B13	B13
—	AN28	P	AN28	eQADC analog input	I	AE	V_{DDA_A0}	AN28	AN28	A13	A13
—	AN29	P	AN29	eQADC analog input	I	AE	V_{DDA_A0}	AN29	AN29	B14	A14
—	AN30	P	AN30	eQADC analog input	I	AE	V_{DDA_B1}	AN30	AN30	C14	B14
—	AN31	P	AN31	eQADC analog input	I	AE	V_{DDA_B1}	AN31	AN31	D14	C14
—	AN32	P	AN32	eQADC analog input	I	AE	V_{DDA_B1}	AN32	AN32	A14	B15
—	AN33	P	AN33	eQADC analog input	I	AE	V_{DDA_B0}	AN33	AN33	B15	D14
—	AN34	P	AN34	eQADC analog input	I	AE	V_{DDA_B0}	AN34	AN34	C15	C15

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
—	AN35	P	AN35	eQADC analog input	I	AE	V_{DDA_B0}	AN35	AN35	D15	D15
—	AN36	P	AN36	eQADC analog input	I	AE	V_{DDA_B1}	AN36	AN36	A15	A15
—	AN37	P	AN37	eQADC analog input	I	AE	V_{DDA_B0}	AN37	AN37	C16	C17
—	AN38	P	AN38	eQADC analog input	I	AE	V_{DDA_B0}	AN38	AN38	C17	D16
—	AN39	P	AN39	eQADC analog input	I	AE	V_{DDA_B0}	AN39	AN39	D16	C16
—	ANB0	P	ANB0	eQADC B shared analog input	I	AE/up-down	V_{DDA_B0}	ANB0	ANB0	C18	C18
—	ANB1	P	ANB1	eQADC B shared analog input	I	AE/up-down	V_{DDA_B0}	ANB1	ANB1	D17	D17
—	ANB2	P	ANB2	eQADC B shared analog input	I	AE/up-down	V_{DDA_B0}	ANB2	ANB2	D18	D18
—	ANB3	P	ANB3	eQADC B shared analog input	I	AE/up-down	V_{DDA_B0}	ANB3	ANB3	D19	D19
—	ANB4	P	ANB4	eQADC B shared analog input	I	AE/up-down	V_{DDA_B0}	ANB4	ANB4	C19	B19
—	ANB5	P	ANB5	eQADC B shared analog input	I	AE/up-down	V_{DDA_B0}	ANB5	ANB5	C20	A20
—	ANB6	P	ANB6	eQADC B shared analog input	I	AE/up-down	V_{DDA_B0}	ANB6	ANB6	B19	C20
—	ANB7	P	ANB7	eQADC B shared analog input	I	AE/up-down	V_{DDA_B0}	ANB7	ANB7	A20	C19
—	ANB8	P	ANB8	eQADC B analog input	I	AE	V_{DDA_B0}	ANB8	ANB8	B20	B20
—	ANB9	P	ANB9	eQADC B analog input	I	AE	V_{DDA_B0}	ANB9	ANB9	D20	A21
—	ANB10	P	ANB10	eQADC B analog input	I	AE	V_{DDA_B0}	ANB10	ANB10	B21	B21
—	ANB11	P	ANB11	eQADC B analog input	I	AE	V_{DDA_B0}	ANB11	ANB11	A21	C21
—	ANB12	P	ANB12	eQADC B analog input	I	AE	V_{DDA_B0}	ANB12	ANB12	C21	A22
—	ANB13	P	ANB13	eQADC B analog input	I	AE	V_{DDA_B0}	ANB13	ANB13	D21	B22
—	ANB14	P	ANB14	eQADC B analog input	I	AE	V_{DDA_B0}	ANB14	ANB14	A22	D20
—	ANB15	P	ANB15	eQADC B analog input	I	AE	V_{DDA_B0}	ANB15	ANB15	B22	C22
—	ANB16	P	ANB16	eQADC B analog input	I	AE	V_{DDA_B0}	ANB16	ANB16	C22	D21

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
—	ANB17	P	ANB17	eQADC B analog input	I	AE	V_{DDA_B0}	ANB17	ANB17	A23	D22
—	ANB18	P	ANB18	eQADC B analog input	I	AE	V_{DDA_B0}	ANB18	ANB18	B23	A23
—	ANB19	P	ANB19	eQADC B analog input	I	AE	V_{DDA_B0}	ANB19	ANB19	C23	B23
—	ANB20	P	ANB20	eQADC B analog input	I	AE	V_{DDA_B0}	ANB20	ANB20	D22	C23
—	ANB21	P	ANB21	eQADC B analog input	I	AE	V_{DDA_B0}	ANB21	ANB21	A24	A24
—	ANB22	P	ANB22	eQADC B analog input	I	AE	V_{DDA_B0}	ANB22	ANB22	B24	B24
—	ANB23	P	ANB23	eQADC B analog input	I	AE	V_{DDA_B0}	ANB23	ANB23	A25	E20
—	VRH_A	P	VRH_A	ADC A Voltage reference high	I	VDDINT	V_{RH_A}	VRH_A	VRH_A	A12	A12
—	VRL_A	P	VRL_A	ADC A Voltage reference low	I	VSSINT	V_{RL_A}	VRL_A	VRL_A	A11	A11
—	VRH_B	P	VRH_B	ADC B Voltage reference high	I	VDDINT	V_{RH_B}	VRH_B	VRH_B	A19	A19
—	VRL_B	P	VRL_B	ADC B Voltage reference low	I	VSSINT	V_{RL_B}	VRL_B	VRL_B	A18	A18
—	REFBYPCB	P	REFBYPCB	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB	REFBYPCB	B18	B18
—	REFBYPCA	P	REFBYPCA	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA	REFBYPCA	B11	B11
—	VDDA_A0	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A0}	VDDA_A0	VDDA_A0	A9	A9
—	VDDA_A1	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A1}	VDDA_A1	VDDA_A1	B9	B9
—	REFBYPCA1	P	REFBYPCA1	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA1	REFBYPCA1	A10	A10
—	VSSA_A1	P	VSSA_A	Ground	I	VSSE	V_{SSA_A1}	VSSA_A1	VSSA_A1	B10	B10
—	VDDA_B0	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B0}	VDDA_B0	VDDA_B0	A16	A16
—	VDDA_B1	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B1}	VDDA_B1	VDDA_B1	B16	B16
—	VSSA_B0	P	VSSA_B	Ground	I	VSSE	V_{SSA_B0}	VSSA_B0	VSSA_B0	B17	B17
—	REFBYPCB1	P	REFBYPCB1	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB1	REFBYPCB1	A17	A17
FlexRay											
248	FR_A_TX_ GPIO248	P	FR_A_TX	FlexRay A transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AD4	AD4
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO248	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
249	FR_A_RX_ GPIO249	P	FR_A_RX	FlexRay A receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AE3	AE3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO249	GPIO	I/O						
250	FR_A_TX_EN_ GPIO250	P	FR_A_TX_EN	FlexRay A transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AF3	AF3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO250	GPIO	I/O						
251	FR_B_TX_ GPIO251	P	FR_B_TX	FlexRay B transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AD5	AD5
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO251	GPIO	I/O						
252	FR_B_RX_ GPIO252	P	FR_B_RX	FlexRay B receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AE4	AE4
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO252	GPIO	I/O						
253	FR_B_TX_EN_ GPIO253	P	FR_B_TX_EN	FlexRay B transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)	—/Up (–/– for Rev.1 of the device)	AF4	AF4
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO253	GPIO	I/O						
FlexCAN											
83	CNTXA_TXDA_ GPIO83	P	CNTXA	FlexCAN A transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AF19	AE19
		A1	TXDA	eSCI A transmit	O						
		A2	—	—	—						
		G	GPIO83	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
84	CNRXA_RXDA_GPIO84	P	CNRXA	FlexCAN A receive	I	MH	V_{DDEH4}	—/Up	—/Up	AE19	AD19
		A1	RXDA	eSCI A receive	I						
		A2	—	—	—						
		G	GPIO84	GPIO	I/O						
85	CNTXB_PCSC3_GPIO85	P	CNTXB	FlexCAN B transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AD19	AC19
		A1	PCSC3	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO85	GPIO	I/O						
86	CNRXB_PCSC4_GPIO86	P	CNRXB	FlexCAN B receive	I	MH	V_{DDEH4}	—/Up	—/Up	AC19	AA19
		A1	PCSC4	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO86	GPIO	I/O						
87	CNTXC_PCSD3_GPIO87	P	CNTXC	FlexCAN C transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AF20	AF20
		A1	PCSD3	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO87	GPIO	I/O						
88	CNRXC_PCSD4_GPIO88	P	CNRXC	FlexCAN C receive	I	MH	V_{DDEH4}	—/Up	—/Up	AE20	AE20
		A1	PCSD4	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO88	GPIO	I/O						
246	CNTXD_GPIO246	P	CNTXD	FlexCAN D transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AD20	AD20
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO246	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
247	CNRXD_ GPIO247	P	CNRXD	FlexCAN D receive	I	MH	V_{DDEH4}	—/Up	—/Up	AC20	AC20
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO247	GPIO	I/O						
eSCI											
89	TXDA_ GPIO89	P	TXDA	eSCI A transmit	O	MH	V_{DDEH1}	—/Up	—/Up	M2	K2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO89	GPIO	I/O						
90	RXDA _ GPIO90	P	RXDA	eSCI A receive	I	MH	V_{DDEH1}	—/Up	—/Up	M3	K3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO90	GPIO	I						
91	TXDB_PCSD1_ GPIO91	P	TXDB	eSCI B transmit	O	MH	V_{DDEH1}	—/Up	—/Up	P1	K1
		A1	PCSD1	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO91	GPIO	I/O						
92	RXDB_PCSD5_ GPIO92	P	RXDB	eSCI B receive	I	MH	V_{DDEH1}	—/Up	—/Up	N1	L5
		A1	PCSD5	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO92	GPIO	I/O						
244	TXDC_ETRIG0_ GPIO244	P	TXDC	eSCI C transmit	O	MH	V_{DDEH4}	—/Up	—/Up	AF23	AF23
		A1	ETRIG0	eQADC trigger input	I						
		A2	—	—	—						
		G	GPIO244	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
245	RXDC_ GPIO245	P	RXDC	eSCI C receive	I	MH	V_{DDEH5}	—/Up	—/Up	AD22	AD22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO245	GPIO	I/O						
DSPI											
93	SCKA_PCSC1_ GPIO93	P	SCKA	DSPI A clock	I/O	MH	V_{DDEH3}	—/Up	—/Up	AD8	AB8
		A1	PCSC1	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO93	GPIO	I/O						
94	SINA_PCSC2_ GPIO94	P	SINA	DSPI A data input	I	MH	V_{DDEH3}	—/Up	—/Up	AF7	AE7
		A1	PCSC2	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO94	GPIO	I/O						
95	SOUTA_PCSC5_ GPIO95	P	SOUTA	DSPI A data output	O	MH	V_{DDEH3}	—/Up	—/Up	AD7	AC7
		A1	PCSC5	DSPI C peripheral chip select	O						
		A2	—	—	—						
		G	GPIO95	GPIO	I/O						
96	PCSA0_PCSD2_ GPIO96	P	PCSA0	DSPI A peripheral chip select	I/O	MH	V_{DDEH3}	—/Up	—/Up	AE6	AD6
		A1	PCSD2	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO96	GPIO	I/O						
97	PCSA1_ PCSE0_GPIO97	P	PCSA1	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AC6	AC6
		A1		DSPI E peripheral chip select							
		A2	—	—	—						
		G	GPIO97	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
98	PCSA2_ SOUTE_GPIO98	P	PCSA2	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AC7	AF6
		A1		DSPI E data output							
		A2	—	—	—						
		G	GPIO98	GPIO	I/O						
99	PCSA3_ SINE_GPIO99	P	PCSA3	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AE7	AD7
		A1		DSPI E data input							
		A2	—	—	—						
		G	GPIO99	GPIO	I/O						
100	PCSA4_ SCKE_GPIO100	P	PCSA4	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AE5	AE5
		A1		DSPI E clock							
		A2	—	—	—						
		G	GPIO100	GPIO	I/O						
101	PCSA5_ETRIG1_ GPIO101	P	PCSA5	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AD6	AA8
		A1	ETRIG1	eQADC trigger input	I						
		A2	—	—	—						
		G	GPIO101	GPIO	I/O						
102	SCKB_ GPIO102	P	SCKB	DSPI B clock	I/O	MH	V_{DDEH3}	—/Up	—/Up	AE8	AC8
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO102	GPIO	I/O						
103	SINB_ GPIO103	P	SINB	DSPI B data input	I	MH	V_{DDEH3}	—/Up	—/Up	AE9	AB9
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO103	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
104	SOUTB_ GPIO104	P	SOUTB	DSPI B data output	O	MH	V_{DDEH3}	—/Up	—/Up	AF9	AA10
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO104	GPIO	I/O						
105	PCSB0_PCSD2_ GPIO105	P	PCSB0	DSPI B peripheral chip select	I/O	MH	V_{DDEH3}	—/Up	—/Up	AD9	AF8
		A1	PCSD2	DSPI D peripheral chip select	O						
		A2	—	—	—						
		G	GPIO105	GPIO	I/O						
106	PCSB1_PCSD0_ GPIO106	P	PCSB1	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AC9	AE8
		A1	PCSD0	DSPI D peripheral chip select	I/O						
		A2	—	—	—						
		G	GPIO106	GPIO	I/O						
107	PCSB2_SOUTC_ GPIO107	P	PCSB2	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AF8	AD8
		A1	SOUTC	DSPI C data output	O						
		A2	—	—	—						
		G	GPIO107	GPIO	I/O						
108	PCSB3_SINC_ GPIO108	P	PCSB3	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AD10	AC9
		A1	SINC	DSPI C data input	I						
		A2	—	—	—						
		G	GPIO108	GPIO	I/O						
109	PCSB4_SCKC_ GPIO109	P	PCSB4	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AC8	AF7
		A1	SCKC	DSPI C clock	I/O						
		A2	—	—	—						
		G	GPIO109	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
110	PCSB5_PCSC0_ GPIO110	P	PCSB5	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up	—/Up	AF6	AE6
		A1	PCSC0	DSPI C peripheral chip select	I/O						
		A2	—	—	—						
		G	GPIO110	GPIO	I/O						
235	SCKC_SCK_C_LVDSP_ GPIO235	P	SCKC	DSPI C clock	I/O	MH+ LVDS	V_{DDEH4}	—/Up	—/Up	AD21	AD21
		A1	SCK_C_LVDSP	LVDS+ downstream signal positive output clock	O						
		A2	—	—	—						
		G	GPIO235	GPIO	I/O						
236	SINC_SCK_C_LVDSM_ GPIO236	P	SINC	DSPI C data input	I	MH+ LVDS	V_{DDEH4}	—/Up	—/Up	AE22	AE22
		A1	SCK_C_LVDSM	LVDS– downstream signal negative output clock	O						
		A2	—	—	—						
		G	GPIO236	GPIO	I/O						
237	SOUTC_SOUT_C_LVDSP_ GPIO237	P	SOUTC	DSPI C data output	O	MH+ LVDS	V_{DDEH4}	—/Up	—/Up	AF21	AF21
		A1	SOUT_C_LVDSP	LVDS+ downstream signal positive output data	O						
		A2	—	—	—						
		G	GPIO237	GPIO	I/O						
238	PCSC0_SOUT_C_LVDSM_ GPIO238	P	PCSC0	DSPI C peripheral chip select	I/O	MH+ LVDS	V_{DDEH4}	—/Up	—/Up	AE21	AE21
		A1	SOUT_C_LVDSM	LVDS– downstream signal negative output data	O						
		A2	—	—	—						
		G	GPIO238	GPIO	I/O						
239	PCSC1_ GPIO239	P	PCSC1	DSPI C peripheral chip select	O	MH	V_{DDEH4}	—/Up	—/Up	AC22	AC22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO239	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
240	PCSC2_GPIO240	P	PCSC2	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	AE23	AE23
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO240	GPIO	I/O						
241	PCSC3_GPIO241	P	PCSC3	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	AD23	AD23
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO241	GPIO	I/O						
242	PCSC4_GPIO242	P	PCSC4	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	AF24	AF24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO242	GPIO	I/O						
243	PCSC5_GPIO243	P	PCSC5	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up	—/Up	AE24	AE24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO243	GPIO	I/O						
EBI											
256	D_CS0_ GPIO256	P	D_CS0	EBI chip select 0	O	F	V_{DDE9}	—/Up	—/Up	—	AD9
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO256	GPIO	I/O						
257	D_CS2_D_ADD_DAT31_ GPIO257	P	D_CS2	EBI chip select 2	O	F	V_{DDE8}	—/Up	—/Up	—	U1
		A1	D_ADD_DAT31	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO257	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
258	D_CS3_D_TEA_ GPIO258	P	D_CS3	EBI chip select 3	O	F	V_{DDE8}	—/Up	—/Up	—	T6
		A1	D_TEA	EBI transfer error acknowledge	I/O						
		A2	—	—	—						
		G	GPIO258	GPIO	I/O						
259	D_ADD12_ GPIO259	P	D_ADD12	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	R1
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO259	GPIO	I/O						
260	D_ADD13_ GPIO260	P	D_ADD13	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	R2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO260	GPIO	I/O						
261	D_ADD14_ GPIO261	P	D_ADD14	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	R3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO261	GPIO	I/O						
262	D_ADD15_ GPIO262	P	D_ADD15	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	R4
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO262	GPIO	I/O						
263	D_ADD16_D_ADD_DAT16_ GPIO263	P	D_ADD16	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	R5
		A1	D_ADD_DAT16	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO263	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
264	D_ADD17_D_ADD_DAT17_ GPIO264	P	D_ADD17	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	T5
		A1	D_ADD_DAT17	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO264	GPIO	I/O						
265	D_ADD18_D_ADD_DAT18_ GPIO265	P	D_ADD18	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	T2
		A1	D_ADD_DAT18	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO265	GPIO	I/O						
266	D_ADD19_D_ADD_DAT19_ GPIO266	P	D_ADD19	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	T3
		A1	D_ADD_DAT19	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO266	GPIO	I/O						
267	D_ADD20_D_ADD_DAT20_ GPIO267	P	D_ADD20	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	T4
		A1	D_ADD_DAT20	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO267	GPIO	I/O						
268	D_ADD21_D_ADD_DAT21_ GPIO268	P	D_ADD21	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AB11
		A1	D_ADD_DAT21	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO268	GPIO	I/O						
269	D_ADD22_D_ADD_DAT22_ GPIO269	P	D_ADD22	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AD10
		A1	D_ADD_DAT22	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO269	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
270	D_ADD23_D_ADD_DAT23_ GPIO270	P	D_ADD23	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AE10
		A1	D_ADD_DAT23	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO270	GPIO	I/O						
271	D_ADD24_D_ADD_DAT24_ GPIO271	P	D_ADD24	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AF10
		A1	D_ADD_DAT24	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO271	GPIO	I/O						
272	D_ADD25_D_ADD_DAT25_ GPIO272	P	D_ADD25	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AD11
		A1	D_ADD_DAT25	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO272	GPIO	I/O						
273	D_ADD26_D_ADD_DAT26_ GPIO273	P	D_ADD26	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AE11
		A1	D_ADD_DAT26	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO273	GPIO	I/O						
274	D_ADD27_D_ADD_DAT27_ GPIO274	P	D_ADD27	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AF11
		A1	D_ADD_DAT27	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO274	GPIO	I/O						
275	D_ADD28_D_ADD_DAT28_ GPIO275	P	D_ADD28	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AD12
		A1	D_ADD_DAT28	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO275	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
276	D_ADD29_D_ADD_DAT29_ GPIO276	P	D_ADD29	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AB12
		A1	D_ADD_DAT29	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO276	GPIO	I/O						
277	D_ADD30_D_ADD_DAT30_ GPIO277	P	D_ADD30	EBI address bus	O	F	V_{DDE9}	—/Up	—/Up	—	AE12
		A1	D_ADD_DAT30	Address and data in mux mode.	I/O						
		A2	—	—	—						
		G	GPIO277	GPIO	I/O						
278	D_ADD_DAT0_ GPIO278	P	D_ADD_DAT0	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	P25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO278	GPIO	I/O						
279	D_ADD_DAT1_ GPIO279	P	D_ADD_DAT1	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	P26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO279	GPIO	I/O						
280	D_ADD_DAT2_ GPIO280	P	D_ADD_DAT2	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	N24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO280	GPIO	I/O						
281	D_ADD_DAT3_ GPIO281	P	D_ADD_DAT3	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	N25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO281	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
282	D_ADD_DAT4_ GPIO282	P	D_ADD_DAT4	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	N26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO282	GPIO	I/O						
283	D_ADD_DAT5_ GPIO283	P	D_ADD_DAT5	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	M25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO283	GPIO	I/O						
284	D_ADD_DAT6_ GPIO284	P	D_ADD_DAT6	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	N22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO284	GPIO	I/O						
285	D_ADD_DAT7_ GPIO285	P	D_ADD_DAT7	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	M24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO285	GPIO	I/O						
286	D_ADD_DAT8_ GPIO286	P	D_ADD_DAT8	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	M23
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO286	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
287	D_ADD_DAT9_ GPIO287	P	D_ADD_DAT9	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	M22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO287	GPIO	I/O						
288	D_ADD_DAT10_ GPIO288	P	D_ADD_DAT10	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	L26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO288	GPIO	I/O						
289	D_ADD_DAT11_ GPIO289	P	D_ADD_DAT11	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	L25
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO289	GPIO	I/O						
290	D_ADD_DAT12_ GPIO290	P	D_ADD_DAT12	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	L24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO290	GPIO	I/O						
291	D_ADD_DAT13 _GPIO291	P	D_ADD_DAT13	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	L23
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO291	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
292	D_ADD_DAT14_GPIO292	P	D_ADD_DAT14	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	L22
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO292	GPIO	I/O						
293	D_ADD_DAT15_GPIO293	P	D_ADD_DAT15	EBI data only in non-mux mode. Address and data in mux mode.	I/O	F	V_{DDE10}	—/Up	—/Up	—	K26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO293	GPIO	I/O						
294	D_RD_WR_GPIO294	P	D_RD_WR	EBI read/write	O	F	V_{DDE10}	—/Up	—/Up	—	R26
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO294	GPIO	I/O						
295	D_WE0_GPIO295	P	D_WE0	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	N1
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO295	GPIO	I/O						
296	D_WE1_GPIO296	P	D_WE1	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	P5
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO296	GPIO	I/O						
297	D_OE_GPIO297	P	D_OE	EBI output enable	O	F	V_{DDE10}	—/Up	—/Up	—	P23
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO297	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
298	D_TS_GPIO298	P	D_TS	EBI transfer start	O	F	V_{DDE9}	—/Up	—/Up	—	AE9
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO298	GPIO	I/O						
299	D_ALE_GPIO299	P	D_ALE	EBI Address Latch Enable	O	F	V_{DDE10}	—/Up	—/Up	—	P24
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO299	GPIO	I/O						
300	D_TA_GPIO300	P	D_TA	EBI transfer acknowledge	I/O	F	V_{DDE9}	—/Up	—/Up	—	AF9
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO300	GPIO	I/O						
301	D_CS1_GPIO301	P	D_CS1	EBI chip select	O	F	V_{DDE9}	—/Up	—/Up	—	AB10
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO301	GPIO	I/O						
302	D_BDIP_GPIO302	P	D_BDIP	EBI burst data in progress	O	F	V_{DDE8}	—/Up	—/Up	—	M2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO302	GPIO	I/O						
303	D_WE2_GPIO303	P	D_WE2	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	N2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO303	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
304	D_WE3_GPIO304	P	D_WE3	EBI write enable	O	F	V_{DDE8}	—/Up	—/Up	—	N3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO304	GPIO	I/O						
305	D_ADD9_GPIO305	P	D_ADD9	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	P1
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO305	GPIO	I/O						
306	D_ADD10_GPIO306	P	D_ADD10	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	P2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO306	GPIO	I/O						
307	D_ADD11_GPIO307	P	D_ADD11	EBI address bus	O	F	V_{DDE8}	—/Up	—/Up	—	P3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO307	GPIO	I/O						
Reset and Clocks											
—	RESET	P	RESET	External reset input	I	MH	V_{DDEH1}	RESET/Up	RESET/Up	R2	N5
230	RSTOUT	P	RSTOUT	External reset output	O	MH	V_{DDEH1}	RSTOUT/Low	RSTOUT/ High	A3	A3
211	BOOTCFG0_IRQ2_ GPIO211	P	BOOTCFG0	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	—/Down	—	L4
		A1	IRQ2		I						
		A2	—	—	—						
		G	GPIO211	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
212	BOOTCFG1_IRQ3_ GPIO212	P	BOOTCFG1	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down	—/Down	N2	L3
		A1	IRQ3	External interrupt request	I						
		A2	—	—	—						
		G	GPIO212	GPIO	I/O						
213	WKPCFG_NMI_ GPIO213[10]	P	WKPCFG	Weak pull configuration input	I	MH	V_{DDEH1}	WKPCFG/Up	—/Up	N3	M5
		A1									
		A2	—	—	—						
		G	GPIO213	GPIO	I						
208	PLLCFG0_IRQ4_ GPIO208	P	PLLCFG0	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/Up	—/Up	R3	M3
		A1	IRQ4	External interrupt request	I						
		A2	—	—	—						
		G	GPIO208	GPIO	I/O						
209	PLLCFG1_IRQ5_GPIO209	P	PLLCFG1	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/Up	—/Up	P2	L1
		A1	IRQ5	External interrupt request	I						
		A2	SOUTD	DSPI D data output	O						
		G	GPIO209	GPIO	I/O						
—	PLLCFG2	P	PLLCFG2	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/ Down	—/ Down	P3	L2
—	XTAL	P	XTAL	Crystal oscillator output	O	AE	V_{DD33}	XTAL	XTAL	AC26	AC26
—	EXTAL	P	EXTAL	Crystal oscillator input	I	AE	V_{DD33}	EXTAL	EXTAL	AB26	AB26
229	D_CLKOUT	P	D_CLKOUT	EBI system clock output	O	F	V_{DDE9}	CLKOUT/ Enabled	CLKOUT/ Enabled	—	AF12
214	ENGCLK	P	ENGCLK	EBI engineering clock output Note: EXTCLK (External clock input) selected through SIU register)	O	F	V_{DDE2}	ENGCLK/ Enabled	ENGCLK/ Enabled	AD1	AD1
JTAG and Nexus (see footnote[11] about resets)											
—	$\overline{\text{EVTI}}$	—[12]	EVTI	Nexus event in	I	F	V_{DDE2}	—/Up	EVTI/Up	T4	V1

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location	
										416	516
227	$\overline{EVTO}$ (the BAM uses this pin to select if auto baud rate is on or off)	–[12]	EVTO	Nexus event out	O	F	V_{DDE2}	ABS/Up	EVTO/HI	U1	V2
219	MCKO	–[12]	MCKO	Nexus message clock out	O	F	V_{DDE2}	O/Low	Disabled[13]	T2	U4
220	MDO0_GPIO220	–[12]	MDO0[14]	Nexus message data out	O	F	V_{DDE2}	See Note[15]	See Note[15]	U3	V3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO220	GPIO	I/O						
221	MDO1_GPIO221	–[12]	MDO1[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	U4	W6
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO221	GPIO	I/O						
222	MDO2_GPIO222	–[12]	MDO2[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V1	V4
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO222	GPIO	I/O						
223	MDO3_GPIO223	–[12]	MDO3[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V2	V5
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO223	GPIO	I/O						
75	MDO4_GPIO75	–[12]	MDO4[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V3	W1
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO75	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
76	MDO5_GPIO76	–[12]	MDO5[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	V4	W2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO76	GPIO	I/O						
77	MDO6_GPIO77	–[12]	MDO6[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	W1	W3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO77	GPIO	I/O						
78	MDO7_GPIO78	–[12]	MDO7[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	W2	Y1
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO78	GPIO	I/O						
79	MDO8_GPIO79	–[12]	MDO8[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	W3	W5
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO79	GPIO	I/O						
80	MDO9_GPIO80	–[12]	MDO9[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	Y1	Y2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO80	GPIO	I/O						
81	MDO10_GPIO81	–[12]	MDO10[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	Y2	Y3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO81	GPIO	I/O						

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
82	MDO11_GPIO82	—[12]	MDO11[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	Y3	Y4
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO82	GPIO	I/O						
231	MDO12_GPIO231	—[12]	MDO12[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	AA1	Y5
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO231	GPIO	I/O						
232	MDO13_GPIO232	—[12]	MDO13[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	AA2	AA1
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO232	GPIO	I/O						
233	MDO14_GPIO233	—[12]	MDO14[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	AA3	AA2
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO233	GPIO	I/O						
234	MDO15_GPIO234	—[12]	MDO15[14]	Nexus message data out	O	F	V_{DDE2}	O/Low	—/Down	Y4	AA3
		A1	—	—	—						
		A2	—	—	—						
		G	GPIO234	GPIO	I/O						
224	$\overline{\text{MSEO0}}$	—[12]	MSEO0[14]	Nexus message start/end out	O	F	V_{DDE2}	O/Low	MSEO/HI	U2	U6
225	$\overline{\text{MSEO1}}$	—[12]	MSEO1[14]	Nexus message start/end out	O	F	V_{DDE2}	O/Low	MSEO/HI	T3	U5
226	RDY	—[12]	RDY	Nexus ready output	O	F	V_{DDE2}	O/Low	RDY/HI	R4	U3
—	TCK	—[12]	TCK	JTAG test clock input	I	F	V_{DDE2}	TCK/Down	TCK/Down	AB2	AB2
—	TDI	—[12]	TDI	JTAG test data input	I	F	V_{DDE2}	TDI/Up	TDI/Up	AC2	AC2
228	TDO	—[12]	TDO	JTAG test data output	O	F	V_{DDE2}	TDO/Up	TDO/Up	AB1	AB1
—	TMS	—[12]	TMS	JTAG test mode select input	I	F	V_{DDE2}	TMS/Up	TMS/Up	AB3	AB3

Table 39. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
—	JCOMP	–[12]	JCOMP	JTAG TAP controller enable	I	F	V_{DDE2}	JCOMP/Down	JCOMP/Down	R1	U2
—	TEST	—	TEST	Test mode select (not for customer use)	I	F	V_{DDEH1}	TEST/Down	TEST/Down	B4	B4
—	VDDSYN	—	VDDSYN	Clock synthesizer power input	I/O	VDDE	V_{DDSYN}	VDDSYN	VDDSYN	AD26	AD26
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V_{DDSYN}	VSSSYN	VSSSYN	AA26	AA26
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V_{DDEH1}	VSTBY	VSTBY	M4	M4
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V_{DDREG}	REGSEL	REGSEL	W23	W23
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V_{DDREG}	REGCTL	REGCTL	Y26	Y26
—	VSSFL	—	VSSFL	Tie to V_{SS}	I	VSS	V_{DDREG}	VSSFL	VSSFL	AB25	AB25
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V_{DDREG}	VDDREG	VDDREG	AA25	AA25

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO functionality. For pins that do not have GPIO functionality, this number is the PCR number.

2 The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is not available on all devices and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

3 P/A/G stands for Primary/Alternate/GPIO . This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alternate *n*) and GPIO.

4 Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the SIU_PCRn registers except where explicitly noted.

5 MH = High voltage, medium speed
F = Fast speed
FS = Fast speed with slew
AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)
VHV = Very high voltage

6 VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can connect to a separate 3.3–5.0 V (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

7 All pins are sampled after the internal POR is negated. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high, ABS — Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

8 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

[9] During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

[10] NMI function is selected using the SIU_IREER/SIU_IFEER registers and has priority over any other function on this pin.

[11] Nexus reset is different than system reset; MDO0-11 are enabled in RPM or FPM trace modes, while MDO12-15 are enabled in FPM trace mode only. MSEO and MCKO are also dependent on trace (RPM or FPM) being enabled.

[12] The Nexus pins don’t have a “primary” function as they are not configured by the SIU. The pins are selected by asserting JCOMP and configuring the NPC. SIU values have no effect on the function of these pins once enabled.

[13] MCKO is disabled from reset; it can be enabled from the tool (controlled by Nexus NPC_PCR register).

[14] Do not connect pin directly to a power supply or ground.

[15] While JCOMP is negated, the MDO0 pad is pulled up because of the default values in its SIU PCR. When JCOMP is asserted, the MDO0 pad is enabled as an output and goes low when the system clock is present.

Appendix B Revision History

Table 40 describes the changes made to this document between revisions.

Table 40. Revision History

Revision	Date	Description
Rev 1	5 Aug 2011	Initial customer release
Rev 2	21 Dec 2011	Added information about specs 1a through 1d in the PMC Electrical Specifications table. Updated the footnote reference (changed from [13] to [14]) of spec 18 of the PMC Electrical Specifications table. Updated the Operating Current 5.0 V Supplies @ fsys = 180MHz VDDA Max value (changed from 30 to 50). Updated footnote [1] of the VDD33 Pad Average DC Current table (changed IDDE to IDD33). Updated the pF value of 11 SRC/DSC Fast with Slew Rate (changed from 2.6 to 200) in the Pad AC Specifications (VDDEH = 5.0 V, VDDE = 3.3 V) table. Added a footnote for ANA0-ANA7 ([9]) functions in the “Signal Properties and Muxing Summary” table. Added a footnote for MDO0-MDO15 ([14]) and MSEO0 functions in the “Signal Properties and Muxing Summary” table. Updated figure numbers 25, 27, 29, and 31: Added specs 1-4. Changed the title of the “PFCPR1 Settings” table to “BIUCR1/BIUCR3”. Added a new row “Load” under “Termination” in the “DSPI LVDS Pad Specification” table. Updated the “Max” and “Typical” values of “Delay, Z to Normal”, “Rise/Fall Time”, and “Data Frequency” in the “DSPI LVDS Pad Specification” table. Changed “V_{DDE}” to “V_{DDEH}” in footnote [10] of the “DC Electrical Specifications” table. Made the following changes in the “DSPI Timing” table: • Update the minimum peripheral bus frequencies for “Data Setup Time for Inputs” and “Data Hold Time for Outputs”. • Updated the maximum peripheral bus frequencies for “Data Valid (after SCK edge)”. • Added “Master (LVDS)” information for “Data Valid (after SCK edge)” and “Data Hold Time for Outputs”. Changed the minimum voltage value of the “I/O Supply Voltage (fast I/O pads)” from “1.62 V” to “3.0 V” in the “DC Electrical Specifications” table. Changed “V_{DDE}” values from “1.62 V to 1.98 V” to “3.0 V to 3.6 V” in footnote [1] of the “Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 3.3 V)” table. Removed voltage ranges “1.62 V–1.98 V” and “2.25 V–2.75 V” from “Fast I/O Weak Pull Up/Down Current” in the “DC Electrical Specifications” table.

Table 40. Revision History (continued)

Revision	Date	Description
Rev 3	10 August 2012	Added minimum and maximum “Nominal bandgap reference voltage” values in the “PMC Electrical Specifications” table. Updated the maximum “Medium I/O Output Low Voltage” value (changed from 0.2 x V_{DDEH} to 0.2 x V_{DDEH} and 0.15 x $_{VDDEH}$) in the “DC Electrical Specifications” table, moved reference to the footnote [10] (I_{OH_S} = {11.6} mA and I_{OL_S} = {17.7} mA for {medium} I/O with V_{DDEH} = 4.5 V; I_{OH_S} = {5.4} mA and I_{OL_S} = {8.1} mA for {medium} I/O with VDDEH = 3.0 V) to “0.2 x V_{DDEH}”, and added a new footnote [11](IOL_S=2 mA) to “0.15 x V_{DDEH}”. Updated footnote[9] (I_{OH_F} = {12,20,30,40} mA and I_{OL_F} = {24,40,50,65} mA for {00,01,10,11} drive mode with V_{DDE} = 3.0 V): Removed “I_{OH_F} = {7,13,18,25} mA and I_{OL_F} = {18,30,35,50} mA for {00,01,10,11} drive mode with V_{DDE} = 2.25 V; I_{OH_F} = {3,7,10,16}mA and I_{OL_F} = {12,20,27,35} mA for {00,01,10,11} drive mode with V_{DDE} = 1.62 V”. Added minimum and maximum values to all rows of the “Power Management Control (PMC) Specification” table. Updated the “Accuracy” temperature values in the “Temperature Sensor Electrical Specifications” table: Changed “–40 C to 100 C to 40 C to 150 C, removed the correspnding “Typ” value, removed “100 C to 150 C, and added minimum (10) and maximum (+10) values. Added a new section “ADC Internal Resource Measurements” and moved “Power Management Control (PMC) Specification”, “Standby RAM Regulator Electrical Specifications”, “ADC Band Gap Reference / LVI Electrical Specifications”, and “Temperature Sensor Electrical Specifications” tables to the section. Changed “Minimum Data Retention at 25 °C ambient temperature” to “Minimum Data Retention at 85 °C ambient temperature” in the “Flash EEPROM Module Life” table. Added the following note after “Flash Program and Erase Specifications (Pending Si characterization)” table in the “C90 Flash Memory Electrical Characteristics” section: “The low, mid, and high address blocks of the flash arrays are erased (all bits set to 1) before leaving the factory. Updated the “DSPI LVDS Pad Specification” table: Changed maximum “Load” value from “25” to “32”; minimum values for “Differential Output Voltage SRC=0b00 or 0b11, SRC=0b01, SRC=0b10” from “150, 90, 160” to “215, 170, 260”; “Transmission lines (Differential) to “Termination Resistance”; “Zc” to “RLoad”; and added the following footnote: “The termination resistance spec is not meant to specify the receiver termination requirements. They are there to establish the measurement criteria for the specs in this table. As per the TIA/EIA-644A standard, the LVDS receiver termination resistance can vary from 90 to 132 Ω .
Rev 4	21 January 2016	Added a table “Flash Memory AC Timing Specifications”. Updated the min and max values from -10 and +10 to -20 and +20 for “Accuracy” in the “Temperature Sensor Electrical Specifications” table.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: MPC5676R
Rev. 4
16 Feb 2016