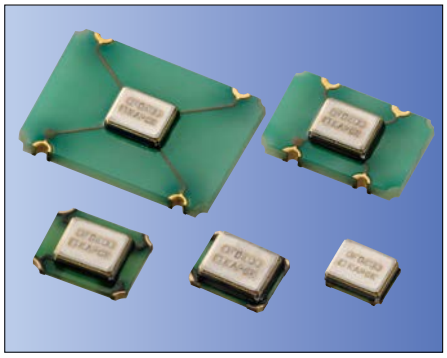
Clock Oscillators Surface Mount Type
Clock "K" Series

KYOCERA

CMOS/ 1.8V, 2.5V, 3.3V, 5.0V Compatible/ 2.0×1.6, 2.5×2.0, 3.2×2.5, 5.0×3.2, 7.0×5.0mm



RoHS Compliant

Features

- Frequency Range 1.5 to 80MHz
- CMOS output
- Wide Supply Voltage 1.6 to 3.63V
- Low current consumption
- Option: Low Phase Noise Version

Applications

- Consumer/ Networking/ Industrial/ Audio Codec/ Amuse

Table 1

Freq. Tol. Code	Freq. Tol. × 10^{-6}	Operating Temperature Range (°C)	Note
0	± 50	−10 to +70	Standard specifications
S	± 30		With only certain frequencies
U	± 25		
G	± 50	−40 to +85	
6	± 50	−40 to +105	

How to Order

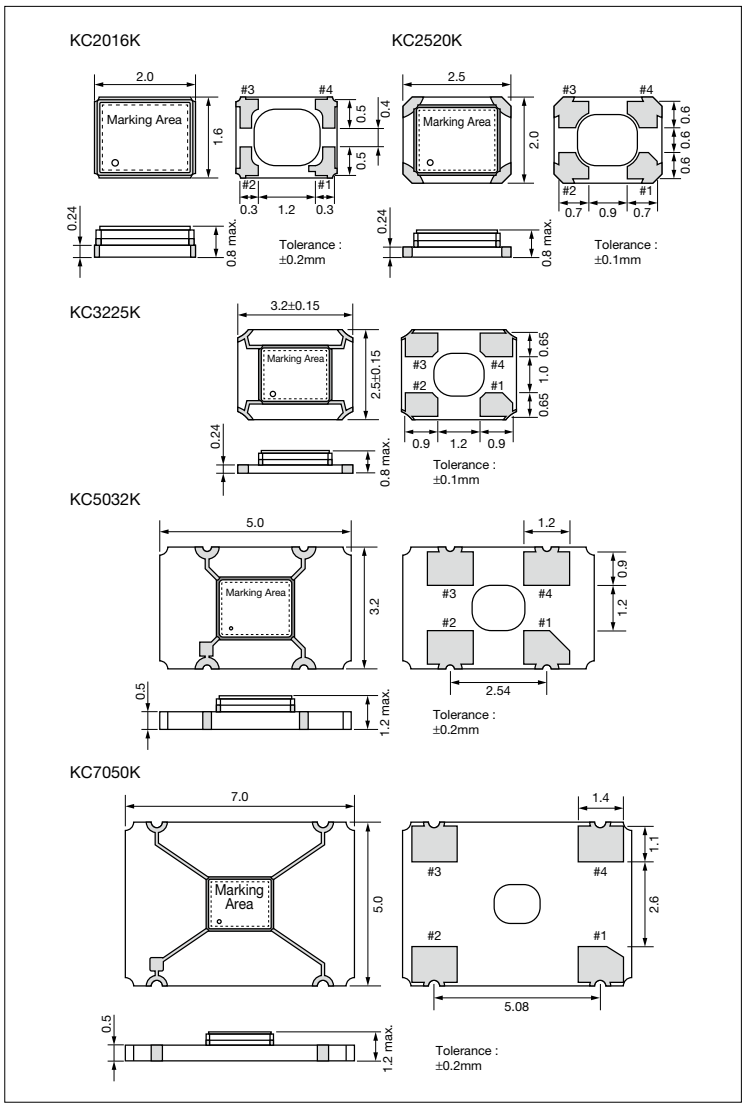
KC2520K 25.0000 C 1 0 E 00
① ② ③ ④ ⑤ ⑥ ⑦

① Series
② Output Frequency (25.0000: 25MHz)
③ Output Type (C: CMOS)
④ Supply Voltage
1 : 1.8V/ 2.5V/ 3.3V Multi Voltage (Version E : Standard)
2 : 2.5V (Version N : Low Phase Noise)
3 : 3.3V (Version N : Low Phase Noise)
5 : 5.0V (Version N : Low Phase Noise)
⑤ Frequency Tolerance (See Table 1)
⑥ Symmetry/ INH Function
E : 45/ 55%, Stand-by
N : 45/ 55%, Stand-by, Low Phase Noise
⑦ Customer Special Model Suffix (STD Specification is "00")

Packaging Tape & Reel
KC7050K/ KC5032K
: 1000 pcs/ reel
KC3225K/ KC2520K/ KC2016K
: 2000 pcs/ reel

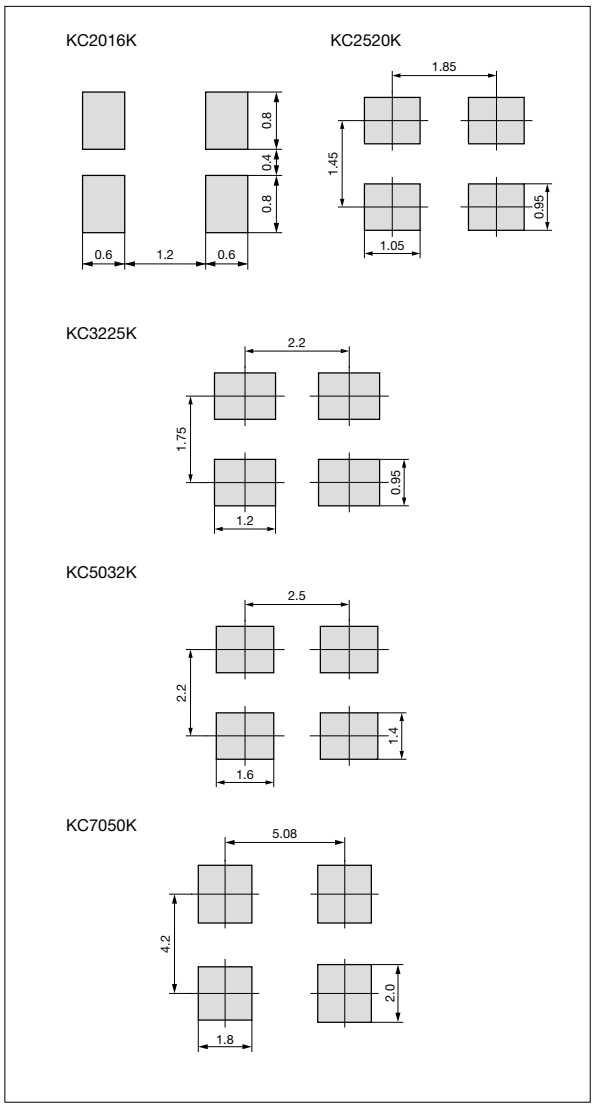
Dimensions

(Unit: mm)



Recommended Land Pattern

(Unit: mm)



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Specifications

Item	Symbol	Conditions		Version E (Standard) Min.	Version E (Standard) Max.	Version N (Low Phase Noise) Min.	Version N (Low Phase Noise) Max.	Units
Output Frequency Range[Note1]	fo			1.5	80	1.5	80	MHz
Frequency Tolerance	f_tol	Initial tolerance, Operating temperature range, Rated power supply voltage change, Load change, Aging (1 year @25°C), Shock and vibration	Op. Temp.: –10 to +70°C/ –40 to +85°C/ –40 to +105°C	–50	+50	–50	+50	×10⁻⁶
			Op. Temp.: –10 to +70°C	–30	+30	–30	+30	
			Op. Temp.: –10 to +70°C	–25	+25	–25	+25	
Frequency Aging	f_age	@25°C First year		–3	+3	–3	+3	×10⁻⁶/ y
Storage Temperature Range	T_stg			–55	+125	–55	+125	°C
Operating Temperature Range	T_use			–10	+70	–10	+70	°C
				–40	+85	–40	+85	
				–40	+105	–40	+105	
Max. Supply Voltage	—			–0.3	+4.0	–0.3	+7.0	V
Supply Voltage	Vcc	Code ④ : 1		+1.60	+3.63	—	—	V
		Code ④ : 2		—	—	+2.25	+2.75	
		Code ④ : 3		—	—	+2.97	+3.63	
		Code ④ : 5		—	—	+4.50	+5.50	
Current Consumption (Maximum Loaded/ 1.5≤F0<24MHz)	Icc	E : 1.6≤Vcc≤2.25V		—	2.5	—	—	mA
		E : 2.25<Vcc≤2.8V/ N : 2.25≤Vcc≤2.75V		—	3.0	—	4	
		E : 2.8<Vcc≤3.63V/ N : 2.97≤Vcc≤3.63V		—	3.5	—	6	
		N : 4.50≤Vcc≤5.50V		—	—	—	24	
Current Consumption (Maximum Loaded/ 24≤F0≤40MHz)		E : 1.6≤Vcc≤2.25V		—	3.5	—	—	
		E : 2.25<Vcc≤2.8V/ N : 2.25≤Vcc≤2.75V		—	4.5	—	5	
		E : 2.8<Vcc≤3.63V/ N : 2.97≤Vcc≤3.63V		—	5.0	—	7	
		N : 4.50≤Vcc≤5.50V		—	—	—	24	
Current Consumption (Maximum Loaded/ 40<F0≤62.5MHz)		E : 1.6≤Vcc≤2.25V		—	5.0	—	—	
		E : 2.25<Vcc≤2.8V/ N : 2.25≤Vcc≤2.75V		—	5.5	—	8	
		E : 2.8<Vcc≤3.63V/ N : 2.97≤Vcc≤3.63V		—	6.0	—	11	
		N : 4.50≤Vcc≤5.50V		—	—	—	24	
Current Consumption (Maximum Loaded/ 62.5<F0≤80MHz)		E : 1.6≤Vcc≤2.25V		—	6.0	—	—	
		E : 2.25<Vcc≤2.8V/ N : 2.25≤Vcc≤2.75V		—	6.5	—	14	
		E : 2.8<Vcc≤3.63V/ N : 2.97≤Vcc≤3.63V		—	8.0	—	18	
		N : 4.50≤Vcc≤5.50V		—	—	—	24	
Stand-by Current	I_std			—	5	—	5	μA
Symmetry	SYM	@50% Vcc		45	55	45	55	%
Rise/ Fall Time (10% to 90% Output Level)	tr/ tf	E : 1.6≤Vcc≤2.25V		—	6	—	—	ns
		E : 2.25<Vcc≤2.8V/ N : 2.25≤Vcc≤2.75V		—	5	—	6	
		E : 2.8<Vcc≤3.63V/ N : 2.97≤Vcc≤3.63V		—	4.5	—	5	
		N : 4.50≤Vcc≤5.50V		—	—	—	8	
Low Level Output Voltage	VOL	E : IOL = 4mA		—	10% Vcc	—	10% Vcc	V
		N (1.5≤Fo≤62.5MHz) : IOL = 4mA						
		N (62.5<Fo≤80MHz) : IOL = 8mA						
High Level Output Voltage	VOH	E : IOH = –4mA		90% Vcc	—	90% Vcc	—	V
		N (1.5≤Fo≤62.5MHz) : IOL = 4mA						
		N (62.5<Fo≤80MHz) : IOL = 8mA						
Output Load	L_CMOS			15[Note2]		15[Note2]		pF
Low Level Input Voltage	VIL			—	30% Vcc	—	30% Vcc	V
High Level Input Voltage	VIH			70% Vcc	—	70% Vcc	—	V
Disable Time	t_dis			—	200	—	150	ns
Enable Time	t_ena			—	3	—	5	ms
Start-up Time	t_str	@Minimum operating voltage to be 0 sec.		—	3	—	5	ms
1 Sigma Jitter	JSigma	Measured with Wavecrest SIA-3000		—	5	—	4	ps
Peak to Peak Jitter	JPK-PK			—	50	—	40	ps
Phase Jitter	JPhase	BW : 12kHz to 20MHz		—	1.0	—	0.3	ps
Phase Noise	—	@25MHz	@10Hz offset	–89		–92		dBc/ Hz
			@100Hz offset	–119		–126		
			@1kHz offset	–143		–151		
			@10kHz offset	–157		–160		
			@100kHz offset	–160		–167		
			@1MHz offset	–162		–170		
			@10MHz offset	–162		–170		

Note: All electrical characteristics are defined at the maximum load and operating temperature range.
Note1: Please contact us for inquiry about operating temperature range, available frequencies and other conditions.
Note2: Please contact us for Output Load 30pF.

Pad Connections	
#1	Enable/ Disable
#2	Case GND
#3	Output
#4	Vcc

INH Function	
Pad1	Pad3 (Output)
Open	Active
"H" Level	Active
"L" Level	High Z (No-Oscillation)