ASG-D Series





7.0 x 5.0 x 1.9mm

FEATURES:

- ASG series is a High Performance crystal based oscillator; available either as an XO or a VCXO
- Frequency range from 10MHz to 250MHz with LVCMOS output
- Available from 10MHz to 1.50GHz with LVDS or LVPECL output
- Offered with either 2.50V or 3.30V bias voltage
- Quick turn, 1~5 business days for small quantity orders

> APPLICATIONS:

- Networking, SONET/SDH
- WiMax / WLAN
- Computing
- Phase Locked Loops
- Direct Digital Synthesis (DDS)
- DSL/ADSL
- · Base Terminal Stations

STANDARD SPECIFICATIONS:

Parameters		Minimum	Typical	Maximum	Units	Notes	
Frequency Range:		$V_{dd} = 3.3V$	10		1500	MHz	
		$V_{dd} = 2.5V$	10		1500	MHz	
Operating Temperature:		-40		+85	°C		
Storage Temperature:		-55		+125	°C		
Overall Frequency Stability:		-50		+50	ppm	See Note # 1	
Initial Set Tolerance		-5.00	≤±1.00	+5.00	ppm		
Stability over operating temperature		-35.00	≤±20.00	+35.00	ppm		
Aging @ 25°C over 10-years		-7.00		+7.00	ppm		
Frequency variation over supply voltage change (±5%)		-2.00		+2.00	ppm		
Frequency variation over load variation $(15pF \pm 5\%)$		-1.00		+1.00	ppm		
Supply Voltage (V	/dd):	$V_{dd} = 3.3V$	3.135	3.300	3.465	V	
Supply Voltage (vuu).	$V_{dd} = 2.5V$	2.375	2.500	2.625	V	
Input Current: $ V_{dd} = 3.3V $ $V_{dd} = 2.5V $		$V_{dd} = 3.3V$		< 25	40	mA	Frequency dependent
				< 25	35	mA	Frequency dependent
	Differential Output Voltage		175	350		mV	$ m V_{OD}$
	V _{OD} Magnitude Change				50	mV	$\Delta { m V}_{ m OD}$
LVDS Output	Offset Voltage			1.25		V	V_{OS}
(Out & <i>Out</i>):	V _{OS} Magnitude Change				50	mV	$\Delta { m V}_{ m OS}$
	Duty Cycle		45	48/52	55	%	ODC_{LVDS}
	Rise Time		125		350	ps	t_R
	Fall Time		150		450	ps	$t_{\scriptscriptstyle \mathrm{F}}$
Start-up Time:			<u>≤</u> 2.0	3.0	ms		
Enable/Disable Function :			"1" ($V_{IH} \ge 0.7*Vdd$) or Open: Oscillation "0" ($V_{IL} < 0.3*Vdd$) : High Z				
Vcontrol Range			0.00		Vdd	Volts	For VCXO
Frequency Pull			±50			ppm	
Control Port Bandwidth			10			kHz	
Integer Mode			< 0.60	1.60	ps	12kHz to 20MHz	
Phase jitter RMS [tjit(\$\phi\$)] Fractional Mode			< 0.90	1.60	ps	12kHz to 20MHz	

Note #1: Inclusive of initial tolerance at 25°C±3°C, operating temperature range, input voltage variation, load variation & aging. Note #2: The rms jitter over 12kHz to 20MHz Bandwidth is dependent on the carrier and whether or not the final frequency is achieved without engaging the Fractional Mode

ABRACON IS ISO9001:2008 CERTIFIED

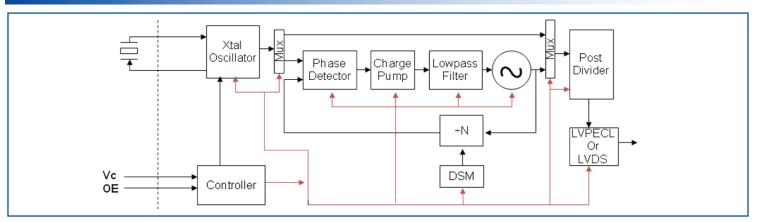


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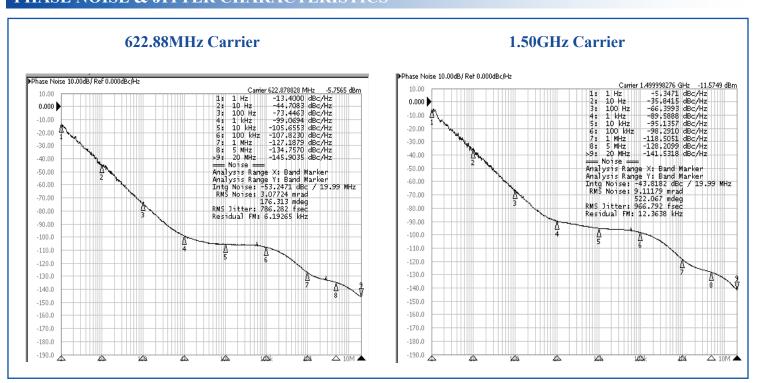




OVERALL SYSTEM BLOCK DIAGRAM



PHASE NOISE & JITTER CHARACTERISTICS





ASG-D Series

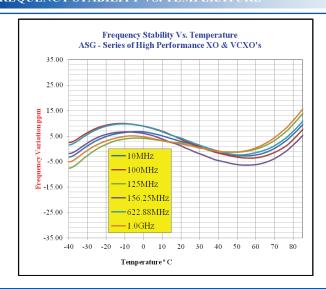


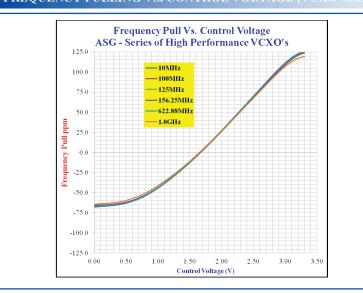


7.0 x 5.0 x 1.9mm

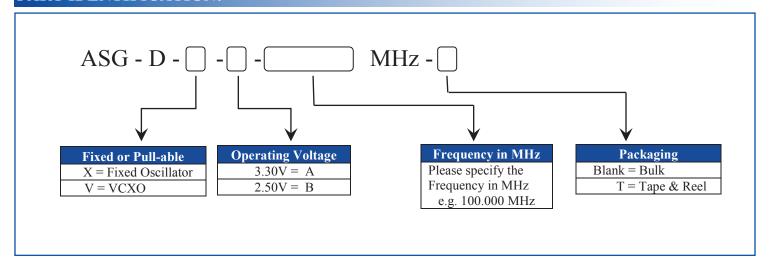
FREQUENCY STABILITY VS. TEMPERATURE

FREQUENCY PULLING VS. CONTROL VOLTAGE (VCXO MODE)

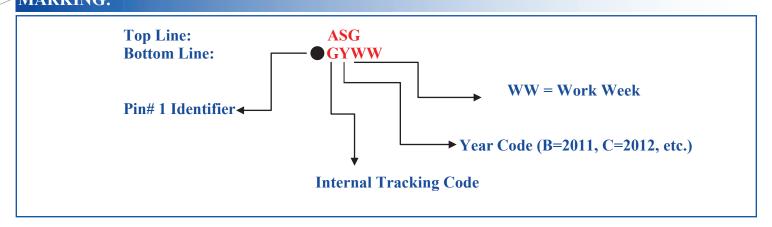




> PART IDENTIFICATION:



MARKING:







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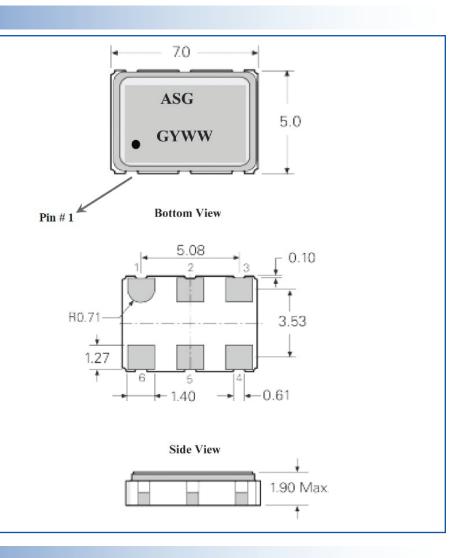




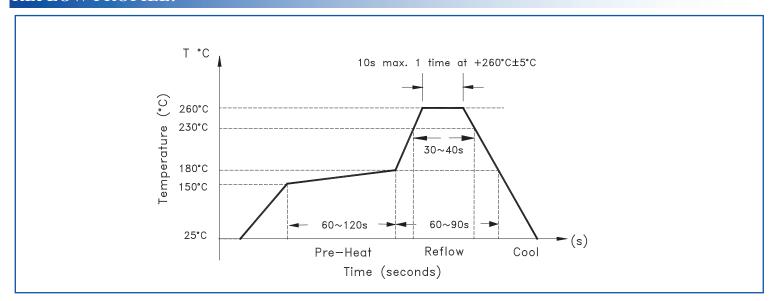
OUTLINE DIMENSIONS:

Pin #	Pin Description For VCXO configuration			
1	Voltage Control for VCXO			
2	Output Enable (OE)			
3	GND			
4	RF Output			
5	RF Output			
6	Vdd			

Pin #	Pin Description For XO configuration
1	Output Enable (OE)
2	N/C for XO
3	GND
4	RF Output
5	RF Output
6	Vdd



REFLOW PROFILE:





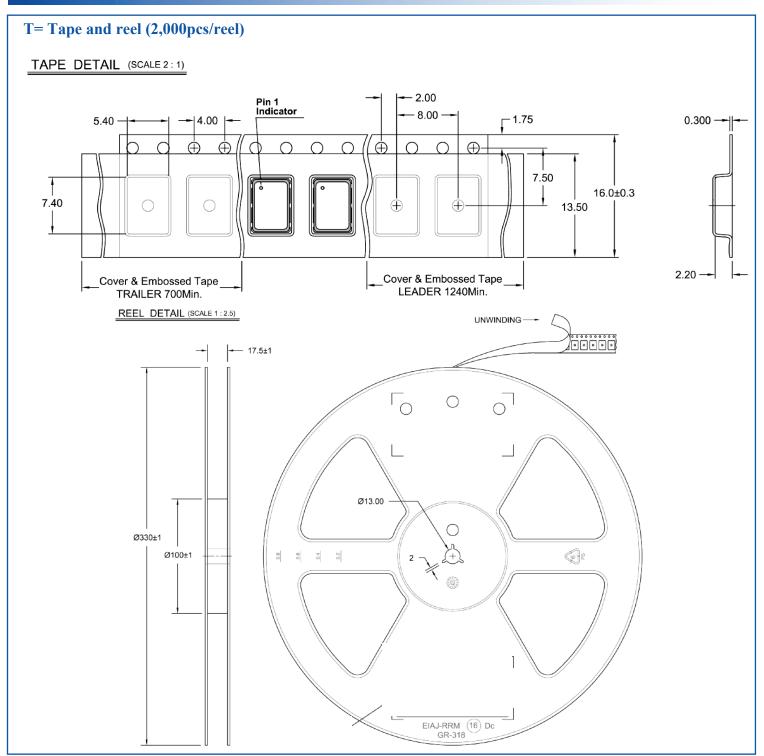


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TAPE & REEL:



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