

Model 638

Ultra Low Jitter LVPECL or LVDS Clock

Features

- Ceramic Surface Mount Package
- Ultra Low Phase Jitter Performance, 100fs Typical
- Fundamental or 3rd Overtone Crystal Design
- Frequency Range 80 – 170MHz *
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418



Part Dimensions:
7.0 × 5.0 × 2.0mm • 178.462mg

Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

Standard Frequencies, 100fs Maximum

- 125.00MHz	- 156.25MHz
- 150.00MHz	- 156.2539MHz
- 155.52MHz	- 161.1328MHz

* See Page 8 for additional developed frequencies.
Check with factory for availability of frequencies

Description

CTS Model 638 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M638 has excellent stability and low jitter/phase noise performance.

Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
638	P	XXX or XXXX	3	I	3	T

Code	Output
P	LVPECL - Pin 1 Enable
L	LVDS - Pin 1 Enable
E	LVPECL - Pin 2 Enable
V	LVDS - Pin 2 Enable

Code	Stability
6	±20ppm ²
5	±25ppm
3	±50ppm
2	±100ppm

Code	Voltage
2	+2.5Vdc
3	+3.3Vdc

Code	Frequency
Product Frequency Code ¹	

Code	Temp. Range
A	-10°C to +60°C
C	-20°C to +70°C
I	-40°C to +85°C

Code	Packing
T	1k pcs./reel

Notes:

- 1) Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2) Consult factory for availability of 6I Stability/Temperature combination.

**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

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Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
Supply Voltage	V_{CC}	$\pm 5\%$	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current						
LVPECL	I_{CC}	Maximum Load	-	55	88	mA
LVDS			-	45	66	
Operating Temperature	T_A	-	-20 -40	+25	+70 +85	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-	-40	-	+125	$^{\circ}\text{C}$

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range						
LVPECL	f_O	-		80 - 170		MHz
LVDS				80 - 170		
Frequency Stability [Note 1]	$\Delta f/f_O$	-		20, 25, 50 or 100		\pm ppm
Aging	$\Delta f/f_{25}$	First Year @ +25 $^{\circ}\text{C}$, nominal V_{CC}	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	R_L	Terminated to $V_{CC} - 2.0\text{V}$	-	50	-	Ohms
Output Voltage Levels	V_{OH}	PECL Load, -20 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$	$V_{CC} - 1.025$	-	$V_{CC} - 0.880$	V
	V_{OL}		$V_{CC} - 1.810$	-	$V_{CC} - 1.620$	
	V_{OH}	PECL Load, -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	$V_{CC} - 1.085$	-	$V_{CC} - 0.880$	V
	V_{OL}		$V_{CC} - 1.830$	-	$V_{CC} - 1.555$	
Output Duty Cycle	SYM	@ $V_{CC} - 1.3\text{V}$	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, $R_L = 50$ Ohms	-	0.3	0.7	ns
LVDS						
Output Type	-	-		LVDS		-
Output Load	R_L	Between Outputs	-	100	-	Ohms
Output Voltage Levels	V_{OH}	LVDS Load	-	1.43	1.60	V
	V_{OL}		0.90	1.10	-	
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	V_{OD}	$R_L = 100$ Ohms	247	330	454	mV
Offset Voltage	V_{OS}	LVDS Load	1.125	1.25	1.375	V
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, $R_L = 100$ Ohms	-	0.4	0.7	ns

Electrical Specifications

Output Parameters

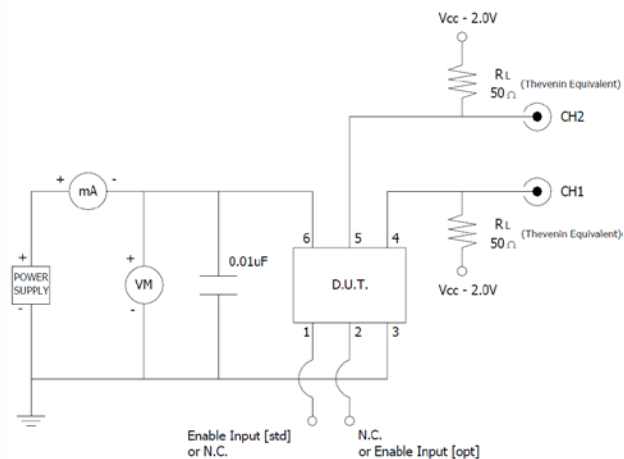
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	T_S	Application of V_{CC}	-	2	5	ms
Enable Function [Standby]						
Enable Input Voltage	V_{IH}	Pin 1 or 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Time	T_{PLZ}	Pin 1 or 2 Logic '0', Output Disabled	-	-	200	ns
Enable Time	T_{PLZ}	Pin 1 or 2 Logic '1', Output Enabled	-	-	2	ms
Phase Jitter, RMS	t_{jrms}	80 - 124.9MHz, Bandwidth 12 kHz - 20 MHz	-	-	200	fs
		125 - 170MHz, Bandwidth 12 kHz - 20 MHz	-	-	100	fs
Period Jitter, pk-pk	p_{jpk-pk}	-	-	2.6	-	ps
Period Jitter, RMS	p_{jrms}	-	-	25	-	ps

Enable Truth Table

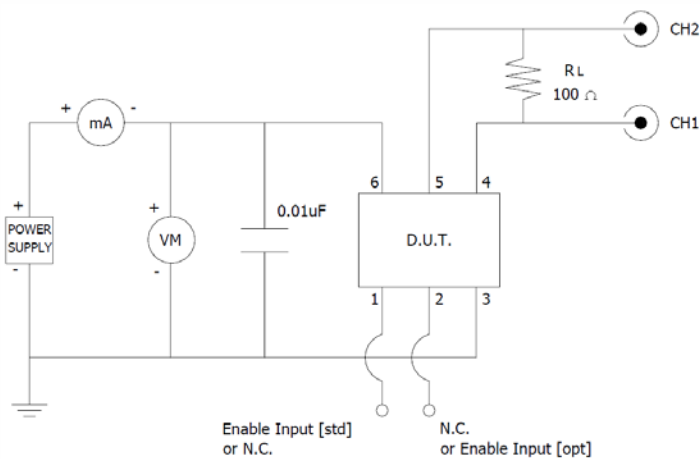
Pin 1 or Pin 2	Pin 4 & Pin 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

Test Circuit

LVPECL

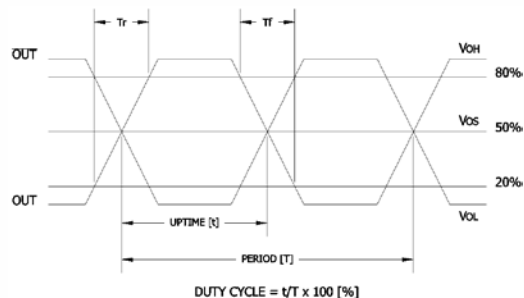


LVDS



Output Waveform

LVPECL or LVDS

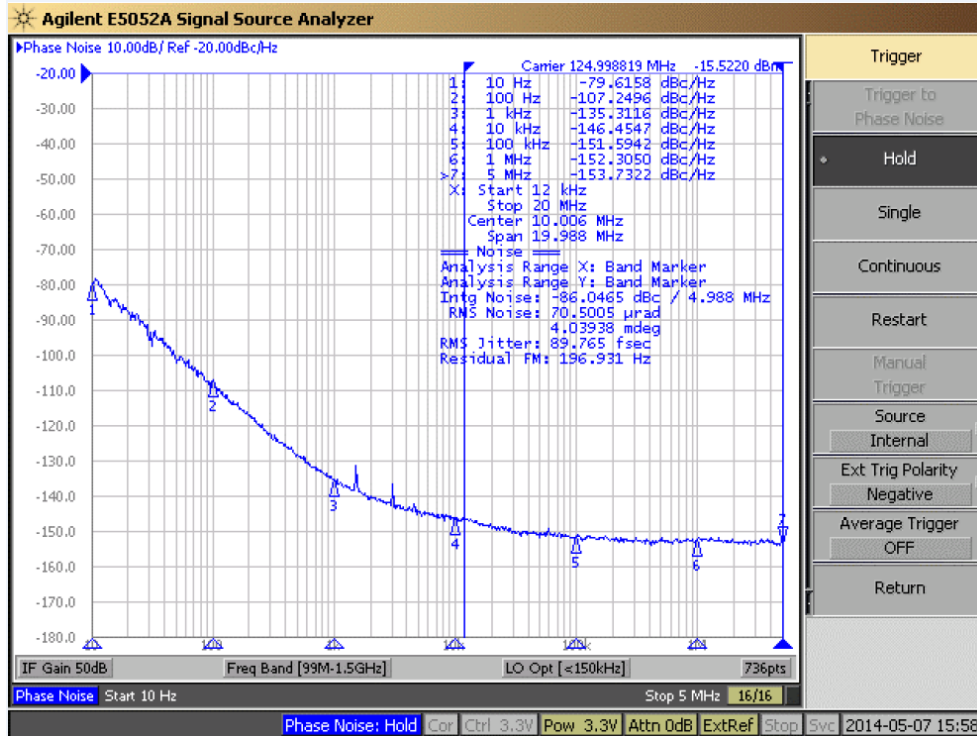


Electrical Specifications

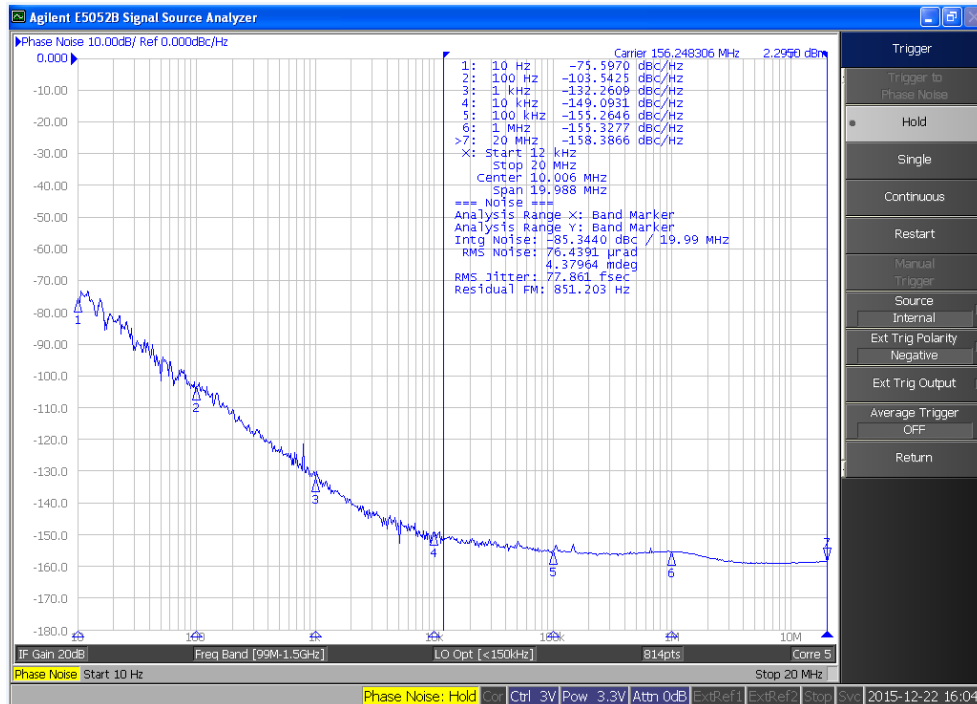
Performance Data

Phase Noise [typical]

125.00MHz, LVPECL, $V_{CC} = 3.3V$, $T_A = +25^\circ C$



156.25MHz, LVPECL, $V_{CC} = 3.3V$, $T_A = +25^\circ C$

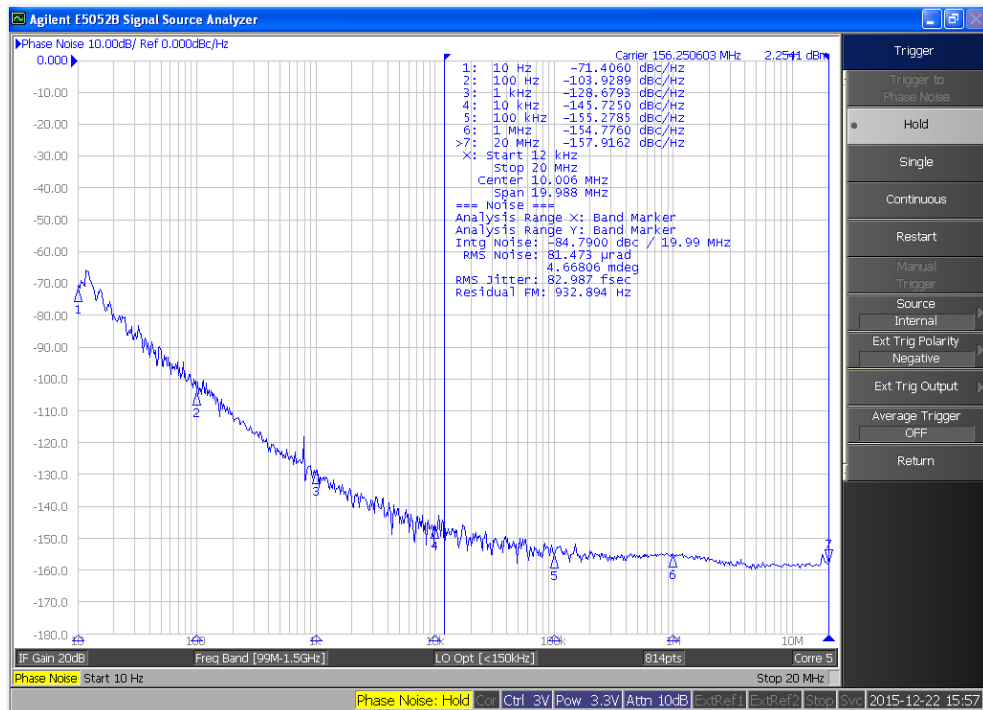


Electrical Specifications

Performance Data

Phase Noise [typical]

156.25MHz, LVDS, $V_{CC} = 3.3V$, $T_A = +25^\circ C$



Phase Noise Tabulated

Typical, $V_{CC} = 3.3V$, $T_A = +25^\circ C$

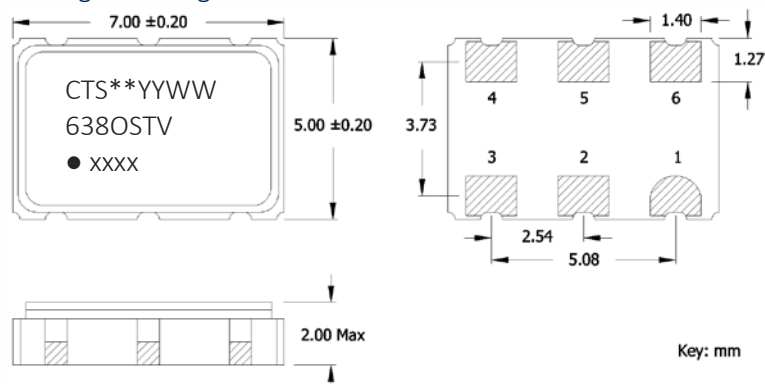
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 125.00MHz				
Phase Noise	-	Single Side Band		
		@ 10Hz	-79.62	dBc/Hz
		@ 100Hz	-107.25	
		@ 1kHz	-135.31	
		@ 10kHz	-146.45	
		@ 100kHz	-151.59	
		@ 1MHz	-152.31	
@ 5MHz	-153.73			
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	89.77	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 156.25MHz				
Phase Noise	-	Single Side Band		
		@ 10Hz	-75.60	dBc/Hz
		@ 100Hz	-103.54	
		@ 1kHz	-132.26	
		@ 10kHz	-149.09	
		@ 100kHz	-155.26	
		@ 1MHz	-155.33	
@ 20MHz	-158.39			
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	77.86	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVDS @ 156.25MHz				
Phase Noise	-	Single Side Band		
		@ 10Hz	-71.41	dBc/Hz
		@ 100Hz	-103.93	
		@ 1kHz	-128.68	
		@ 10kHz	-145.73	
		@ 100kHz	-155.28	
		@ 1MHz	-154.78	
@ 20MHz	-157.92			
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	82.99	fs

Mechanical Specifications

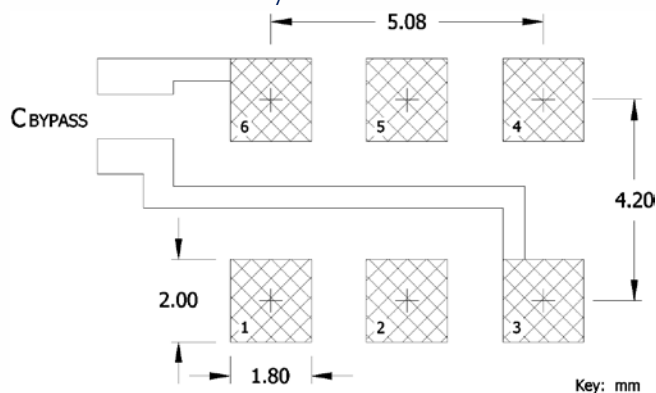
Package Drawing



Marking Information

- ** - Manufacturing Site Code.
- YYWW – Date Code; YY – year, WW – week.
- O – Output Type; P or E = LVPECL, L or V = LVDS.
- ST – Frequency Stability/Temperature Code.
[Refer to Ordering Information]
- V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
- xxxx – Frequency Code.
3-digits, frequencies below 100MHz
4-digits, frequencies 100MHz or greater
[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

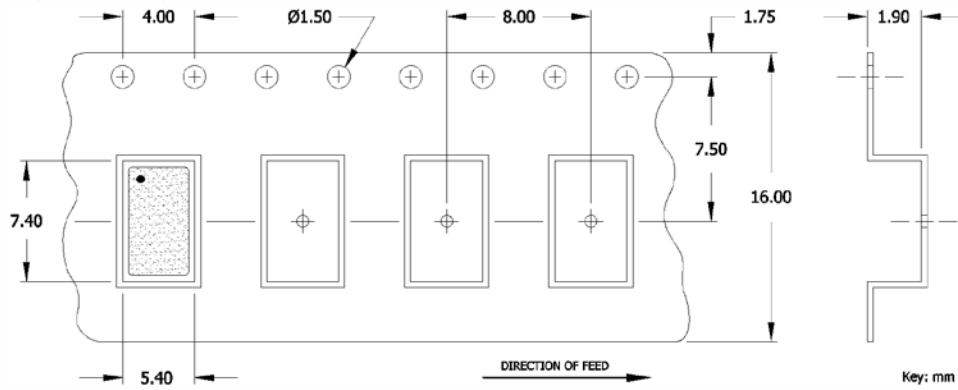
- JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

Pin Assignments

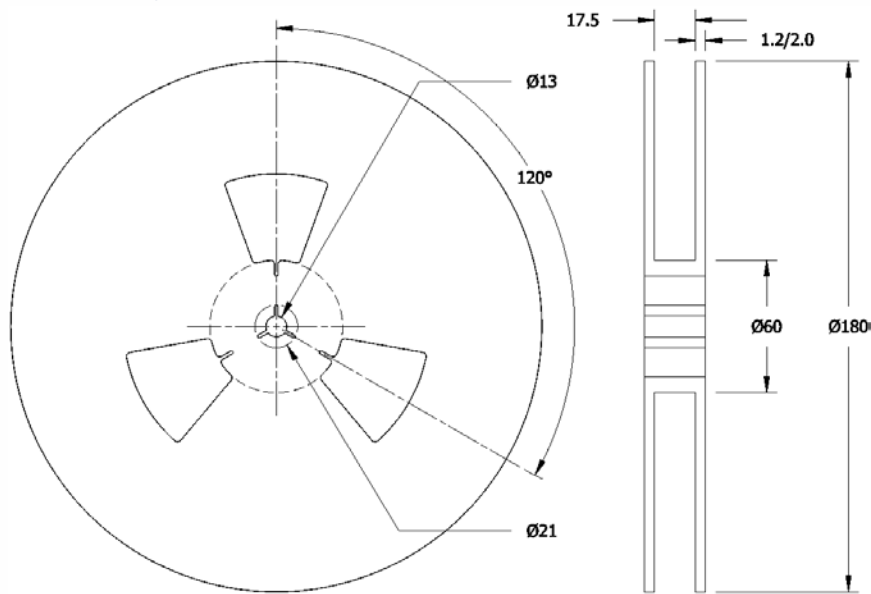
Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V _{CC}	Supply Voltage

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.



Addendum

Additional Developed Frequencies – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
80.000000	800						
100.000000	1000						
120.000000	1200						
133.000000	1330						
148.351600	148A						
148.500000	1485						
153.600000	1536						
156.253906	156A						
167.372800	167A						

Frequency Codes for Cover Page Table – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
125.000000	1250	156.253900	156E				
150.000000	1500	161.132800	1611				
155.520000	1555						
156.250000	1562						