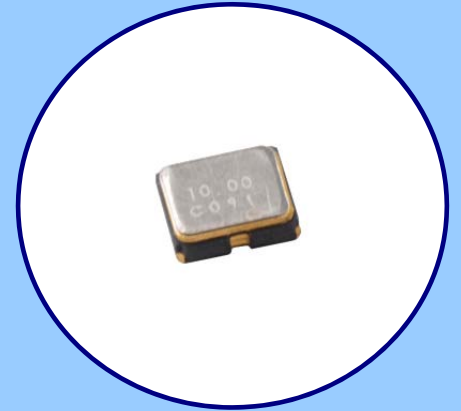




FEATURES

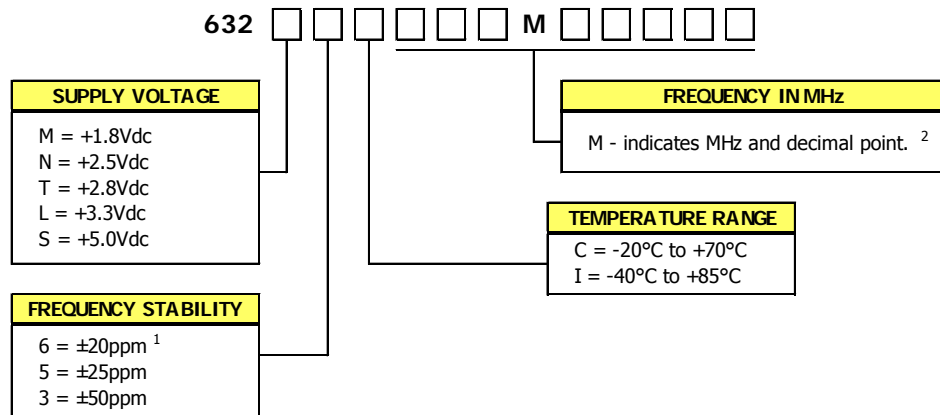
- Standard 3.2mm x 2.5mm 4-Pad Surface Mount Package
- HCMOS Output
- Fundamental and 3rd Overtone Crystal Designs
- Frequency Range 1 – 125 MHz
- Frequency Stability ±50 ppm Standard, ±25 ppm and ±20 ppm Available
- Operating Voltages +1.8Vdc, +2.5Vdc, +2.8Vdc, +3.3Vdc or +5.0Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



APPLICATIONS

Model 632 is ideal for applications; such as broadband access, Ethernet/Gigabit Ethernet, microprocessors/DSP/FPGA, networking equipment computers and peripherals, digital video, cameras and other portable devices.

ORDERING INFORMATION



1] Consult factory for 6l Stability/Temperature availability.

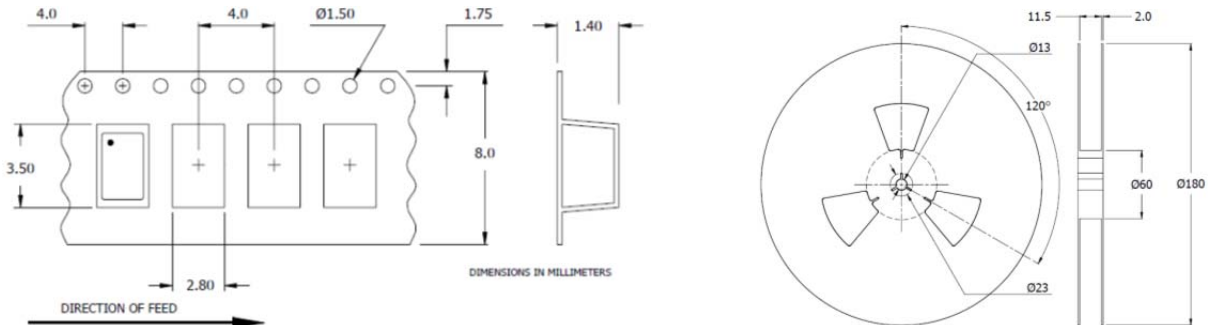
2] Frequency is recorded with three leading significant digits before the 'M' and 5 significant digits after the 'M' [including zeros].

[Ex. 3.579545 MHz, code as 003M57954; 14.31818 MHz, code as 014M31818; 125 MHz, code as 125M00000]

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. minimum and 3k pcs. maximum per 180mm reel. **8mm tape width.**



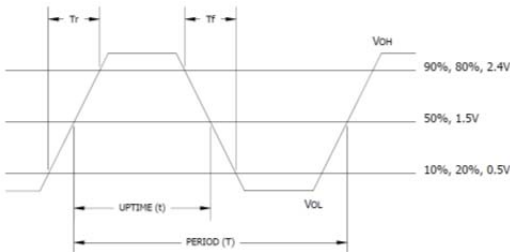
ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	4.0	V
Storage Temperature	T_{STG}	-	-40	-	+100	°C
Frequency Range	f_0	-	1.0	-	125	MHz
Frequency Stability [See Note 1 and Ordering Information]	$\Delta f/f_0$	-	-	-	20, 25, 50	± ppm
Aging	$\Delta f/f_0$	-	-	-	3	± ppm/yr
Operating Temperature Commercial Industrial	T_A	-	-20 -40	+25	+70 +85	°C
Supply Voltage Model 632M Model 632N Model 632T Model 632L Model 632S	V_{CC}	± 10 %	1.62 2.25 2.52 2.97 4.50	1.8 2.5 2.8 3.3 5.0	1.98 2.75 3.08 3.63 5.50	V
Supply Current Model 632M [+1.8V] Model 632N, 632T [+2.5V, +2.8V] Model 632L, 632S [+3.3V, +5.0V]	I_{CC}	$C_L = 15\text{pF}$ 1.0 MHz to 100 MHz 100.1 MHz to 125 MHz 1.0 MHz to 100 MHz 100.1 MHz to 125 MHz 1.0 MHz to 100 MHz 100.1 MHz to 125 MHz	- - - - - -	- - - - - -	7 12 10 20 15 25	mA
Output Load	C_L	-	-	-	15	pF
Output Voltage Levels Logic '1' Level Logic '0' Level	V_{OH} V_{OL}	CMOS Load CMOS Load	90% V_{CC} -	- -	- 10% V_{CC}	V
Output Current Logic '1' Level [M,N,T,L,S] Logic '0' Level [M,N,T,L,S]	I_{OH} I_{OL}	$V_{OH} = 90\%V_{CC}$ [1.8V, 2.5/2.8V, 3.3V, 5.0V] $V_{OL} = 10\%V_{CC}$ [1.8V, 2.5/2.8V, 3.3V, 5.0V]	- -	- -	-2, -4, -8, -16 +2, +4, +8, +16	mA
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time Model 632M [+1.8V] Model 632N, 632T [+2.5V, +2.8V] Model 632L, 632S [+3.3V, +5.0V]	T_R, T_F	@ 10% - 90% Levels, $C_L = 15\text{pF}$ 1.0 MHz to 20 MHz 20.1 MHz to 125 MHz 1.0 MHz to 20 MHz 20.1 MHz to 125 MHz 1.0 MHz to 20 MHz 20.1 MHz to 125 MHz	- - - - - -	- - - - - -	5 4 4 3 3 2	ns
Start Up Time	T_S	Application of V_{CC}	-	-	2	ms
Enable Function Enable Input Voltage Disable Input Voltage	V_{IH} V_{IL}	Pin 1 Logic '1', Output Enabled Pin 1 Logic '0', Output Disabled	0.7* V_{CC} -	- -	- 0.3* V_{CC}	V
Enable Time [M,N,T,L,S]	T_{PLZ}	Pin 1 Logic '1'	-	-	2	ms
Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	15	µA
Period Jitter, pk-pk	pjpk-pk	-	-	-	40	ps
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	-	1	ps

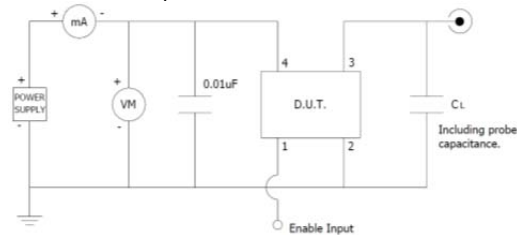
Notes:

- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and aging.

LVC MOS OUTPUT WAVEFORM



TEST CIRCUIT, CMOS LOAD

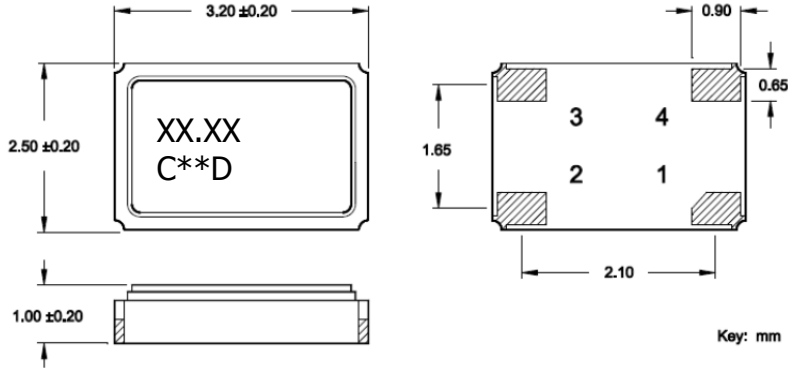


ENABLE TRUTH TABLE

PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

1. XX.XX – Frequency in MHz.
2. C – CTS and Pin 1 identifier.
3. ** - Manufacturing Site Code.
4. D – Manufacturing Date Code.
[See Table 1 for codes.]
5. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.

NOTES

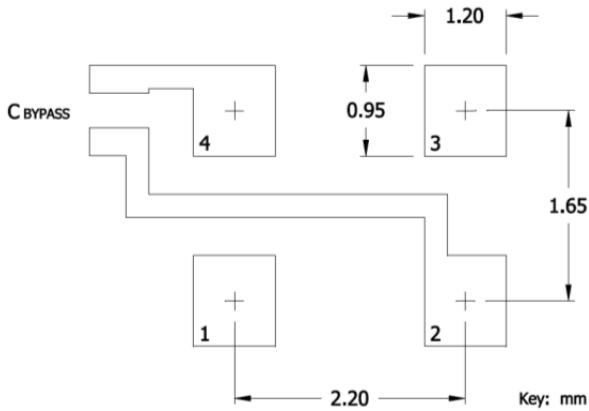
1. Termination pads (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
3. MSL = 1.

TABLE I

YEAR					MONTH											
					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.



D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V _{CC}	Supply Voltage